TÉCNICO LISBOA

Vector Network Analyser – Signal Generation

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Thesis to obtain the Master of Science Degree in

Electronics Engineering

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May 2016

Abstract

As fast electronics continues to expand, the demand to test and characterize such type of circuitry becomes even more common. With the necessity of higher bandwidths the frequency will naturally increase, resulting in short wavelengths. Some of the signals tend to have the same order of the dimension of the electrical components, which means that the electrical network should be analyzed with distributed elements. For this situation, measuring the magnitude and phase of transmitted and reflected signals offers the only method to characterize a microwave circuit, so such characterization requires a Vector Network Analyzer.

This dissertation work focuses on developing various prototype modules with the purpose to test some fundamental circuitry that composes a Vector Network Analyzer. A programmable wide-band microwave signal source with phase tuning capability, with a bandwidth of 35 MHz to 4.4 GHz and respective frequency extender, up to 16 GHz, prototype modules were fabricated and tested. With the obtained results, an architecture study is proposed for the signal generator module with 4 output bands, covering from 54 MHz to 24 GHz of bandwidth. Not all aspects were covered since it requires considerable time and effort to develop a fully functional instrument for measuring a significant band, 54 MHz to 24 GHz.

Keywords

Transmission line, Wide band signal source, Frequency doublers, Sampling in VNAs.

Resumo

À medida que a electrónica rápida se expande, a necessidade de testar e caracterizar circuitos em micro-ondas torna-se cada vez mais importante. Para se atingir larguras de banda elevadas é necessário que a frequência dos sinais também aumente. Tal facto resulta em ondas cada vez mais curtas, o que implica que esses comprimentos sejam da mesma ordem de grandeza dos componentes discretos. Por este motivo, os circuitos têm de ser analisados como elementos distribuídos. Medir a magnitude e a fase do sinal reflectido ou transmitido é o único método de caracterização de um circuito de micro-ondas, só sendo possível com um Analisador de Redes Vectorial.

Este trabalho foca-se no estudo e desenvolvimento de alguns dos circuitos que constituem um Analisador de Redes Vectorial. Desenvolveu-se um protótipo de um gerador de sinais com uma largura de banda de 35 MHz até 4.4 GHz, com a capacidade de ajustar a fase, assim como módulos para expandir a frequência até 16 GHz. Com os resultados obtidos é sugerido um estudo baseado numa possível arquitectura para o gerador de sinais, que tem a possibilidade de cobrir uma banda desde os 54 MHz até os 24 GHz. Nem todos os aspectos foram abordados, dado que a complexidade do trabalho requer bastante tempo para a fabricação de um instrumento completamente funcional, capaz de medir frequências na banda 54 MHz até 24 GHz.

Palavras-chave

Linhas de transmissão, Gerador de sinais, Duplicadores de frequência, Amostragem em VNAs.

Acronyms

ADC	Analog-to-Digital Converter
ADS	Advance Design System
AGC	Automatic Gain Control
CNC	Computer Numeric Control
CPWG	Co Planar Waveguide With Ground
dB	decibels
dBc	Decibels relative to a carrier
dBm	decibel-milliwatts
DC	Direct Current
DDS	Direct Digital Synthesizer
DUT	Device Under Test
EMI	Electromagnetic Interference
FDTD	Finite-Difference Time-Domain
GaAs	Gallium Arsenide
GUI	Graphic User Interface
IF	Intermediate Frequency
MESFET	Metal-semiconductor Field-Effect Transistor
MMIC	Monolithic Microwave Integrated Circuit
NLTL	Non-Linear-Transmission-Lines
OCXO	Oven Controlled Crystal Oscillator
PC	Personal Computer
PCB	Printed Circuit Board
PFD	Phase Frequency Detector
PLL	Phase Locked Loop
PPM	Parts Per Million
RF	Radio Frequency
S-Parameters	Scattering Parameters

SMA	Sub Miniature version A
SMK	Sub Miniature version K
SOLT	Short-Open-Load-Thru
SPI	Serial Peripheral Interface
SRD	Step Recovery Diode
SRF	Self Resonant Frequency
SWR	Standing Wave Ratio
TDR	Time Domain Reflectometer
TEM	Transverse Electromagnetic Mode
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
VNA	Vector Network Analyzer
YIG	Yttrium Iron Garnet
Z0	Characteristic Impedance
Z0even	Characteristic Impedance for the even mode
Z0odd	Characteristic Impedance for the odd mode

Acknowledgments

First of all, would like to thank my supervisors, Professor Maria João Rosário and Professor Moisés Piedade for all the support in this dissertation work, thank you for your disponibility and for sharing knowledge.

A special thanks to João Graça, Jorge Candeias, Ruben Afonso, Mr. Pina dos Santos, Professors João Vaz, Marcelino Santos, Paulo Branco, António Ferraz, Pedro Ramos and all my colleagues of Instituto Superior Técnico.

Some words of gratitude to my sweet girlfriend Joana Silva, thank you my dear for supporting me in all moments.

I would also like to thank all my family members for all the patience and love, especially to my parents and my brothers.

Finally but not least my entire gratitude to GOD, for aiding me in the good and bad moments of my life.

José Dias

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Chapter 1 – Introduction

1.1 – Purpose and motivation

As the number of applications that use microwave electronics grows, the need for measuring and testing at high frequencies will also follow the tendency. Many instruments offer the possibility to test and measure signals, such as oscilloscopes and spectrum analyzers, but this type of instruments doesn't provide complete characterization of circuit network (phase information is missing). Per example to create a wide band Radio Frequency (RF) Choke [1], it is necessary to minimize the presence of the RF signal, on the Direct Current (DC) path, it seems simple but it would be necessary to verify if the characteristic impedance from the transmission line doesn't significantly change once the DC path is inserted. For this type of problems a Vector Network Analyzer (VNA) is a necessary instrument to fully characterize a Device Under Test (DUT).

With the VNA it is possible to measure the magnitude and phase characteristics of networks. By comparing the reflected or transmitted signals from a DUT relative to an incident signal, it is possible to determine all the important performances, such as: phase insertion, group delay, impedance, return loss, Standing Wave Ratio (SWR), gain, transmission coefficients, reflection coefficients [2].

As new and ultra-wideband Monolithic Microwave Integrated Circuit (MMIC) become available at lower prices an opportunity emerges to develop some of the essential circuitry that composes a VNA.

1.2 – Objectives and challenges

The main objective for this dissertation is to develop a functional signal generator prototype that covers a 54 MHz to 24 GHz bandwidth and to study VNA architectures in order to suggest a future work plan. The signal generator was designed considering both VNA receivers architecture, homodyne and heterodyne, however the homodyne solution is the preferable because of the easier implementation.

In order to obtain significant results for the given amount of time 2 objectives were defined as a starting point:

- Develop a wideband signal generator prototype, able to reach a bandwidth up to 4.4 GHz with the capability of adjusting the output phase and power.
- Develop a frequency extender architecture in order to expand the bandwidth of the signal generator prototype, up to 24 GHz.

The challenges of this dissertation work are the ones that are usually found in RF/Microwave engineering: Transmission line adaptation; Maximization of harmonic rejection through filtering and layout techniques; Minimization of phase noise in every section; Finding the right discrete components with high Self Resonant Frequency (SRF) (for designing wide band RF bias tee); Adjustment of the manufacturing process for each prototype module;

Not all aspects will be solved or even addressed, but most of the efforts are directed on the critical sections of signal generation at RF/Microwave frequencies.

1.3 – Document organization

Chapter 2 contains an overview of vector measurements with the basic physics, it also contains a description of the basic circuits needed to a VNA and the respective state-of-the-art of modern architectures. The main objective in the chapter is to transmit to the reader the main modules architecture and advantages between each other.

In chapter 3 a brief study of transmission lines is presented, showing the comparison between two types of lines with measurements up to 24 GHz. It also presents some solutions in order to optimize transmission line when connectors are added.

Chapter 4 presents two wideband signal generators prototypes using the ADF435x synthesizer family. The first signal generator has a total bandwidth of 137,5 MHz to 4.4 GHz and the second covers from 35 MHz to 4.4 GHz, it also presents the control software, using a Personal Computer (PC), and the measured results. It also contains a frequency extension study, 4 prototypes that were designed and tested in order to double/quadruple the total bandwidth of the signal generator prototypes.

The fifth chapter is a suggestion for a signal source architecture that can be studied in order to minimize the total number of components, since some results of the frequency extender didn't allow to cover the entire bandwidth.

As for the final chapter, 6, some conclusions are stated considering the results obtained in this dissertation work and the future work challenges.

Chapter 2 – Vector measurement and VNA basic architecture

2.1 – Introduction to vector measurements

Vector measurements consist on measuring both magnitude and phase of a signal, relative to a reference, it is a very practical way to characterize linear networks and has a great importance in circuit design, per example it can be used to measure complex impedance's of two components and create a matching network for minimize power reflections between the components.

Electrical networks behavior can be predicted when small signals, applied to network ports, cause the network to respond in a linear manner, even if the components of the network are unknown [3]. When an incident traveling wave is applied in one of the network ports, the network will react according with its elements, and two waves appear, the reflected and the transmitted. The same analogy exist when light is reflected and transmitted from a prism as show in figure 1,

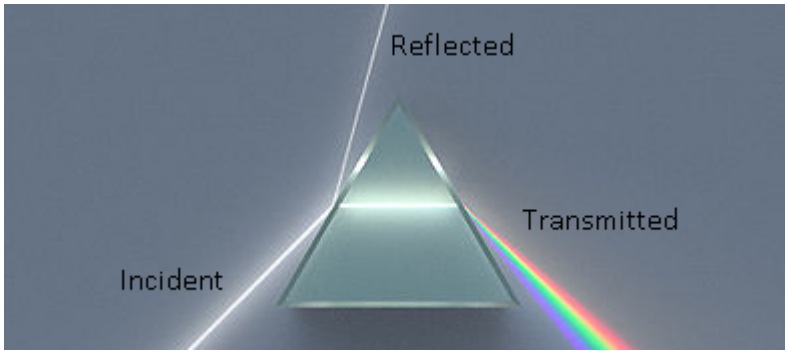


Figure 1 – Lightwave analogy to high-frequency device characterization.

In other words it is possible to characterize a device when the transmission and reflection coefficients are determined. Table 1 describes some of the common terms to describe a device in high frequency.

Table 1 – Common terms to describe a device in high frequency.

Common terms related to transmission	**Common terms related to reflection**
Gain/Loss	Standing Wave Ratio (SWR)
Transmission coefficients	Reflection coefficients
Insertion phase	Reflection coefficients vs time
Electrical length/delay	Impedance (R+jX)
Deviation from linear phase	Admittance (G+JB)
Group delay	Return loss

2.2 – Scattering parameters

VNAs rely on Scattering parameters (S-parameters) in order to characterize networks. Since it isn't no longer possible to define open or short circuits when dealing with distributed elements. Figure 2 illustrates a DUT of two ports and the orientation of the power waves across the DUT.

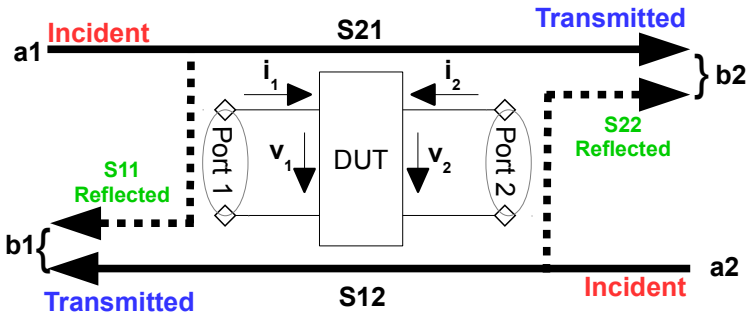


Figure 2 – Power waves on a 2-port network.

The incident waves a_1 and a_2 and the reflected waves b_1 and b_2 are normalized to a specific complex impedance, per example Z_0, each wave is described in [3] by

$$a_i = \frac{v_i + i_i Z_0}{2\sqrt{\mathrm{Re}\{Z_0\}}} \tag{1}$$

$$b_i = \frac{v_i - i_i Z_0^{\,*}}{2\sqrt{\mathrm{Re}\{Z_0\}}} \tag{2}$$

and the relation between power waves on a 2 port network and the S-parameter is given by

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{3}$$

The following table 2 gives the common terms associated for the S-parameter used in engineering.

Table 2 – Common terms for a 2 port S-parameter matrix.

S_{11}	Input reflection coefficient with a matched load
S_{12}	Direct transmission gain with a matched load
S_{21}	Reverse transmission gain with a matched source
S_{22}	Output reflection coefficient with a matched source

2.3 – VNA architecture

A VNA is basically composed by a signal generator which is responsible to generate the incident traveling wave to the DUT, a microwave test-and-set board with switching capability in order to route the stimulus signals to the DUT. At each port of the DUT reflectometer/coupling bridges are used to couple a portion of the incident, reflected and transmitted waves. After the 3 waves are acquired they are down-converted, the digitalization of an analog signal is made by an Analog-to-Digital Converter (ADC). Figure 3 illustrates a generic VNA block diagram.

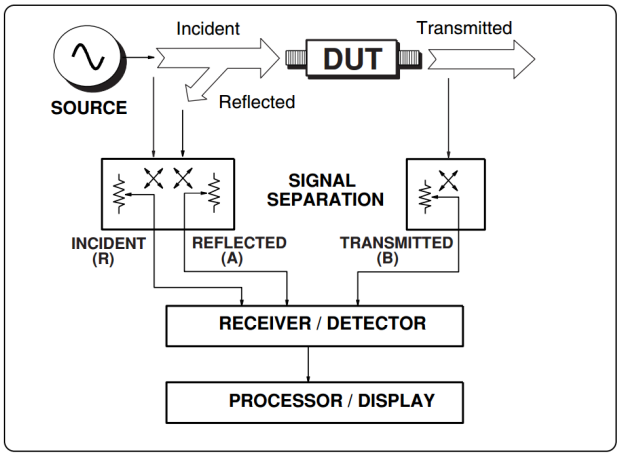


Figure 3 – Generalized VNA block diagram [4].

The following sections 2.3.1 to 2.3.3 summarizes the principles for the signal generators, signal coupling and down-conversion schemes and sampling architectures applied to VNAs. As for the section 2.3.4 a State-of-the-art of modern VNA is presented.

2.3.1 – Signal generator

The signal generator for a VNA produces a microwave stimulus for the DUT, it should be a clean frequency tone with low phase noise and constant power. Phase noise will naturally demote the phase resolution for vector measurements. The speed of the frequency sweep also degrades the phase resolution, especially if it is a fast sweep, per example an analog-sweep which is a signal that isn't locked. A step-sweep should be used in order to improve phase resolution even if it is slower, since it is locked to a phase loop [2].

A signal generator based in a Phase Locked Loop (PLL) architecture is basically composed by a fixed low phase noise reference section, per example an Oven Controlled Crystal Oscillator (OCXO), the PLL synthesizer which is responsible to translate the reference frequency to a new frequency with a wide band tunable Voltage Controlled Oscillator (VCO) or a Yttrium Iron Garnet (YIG) oscillator. A VCO allows a faster sweep time but it has a higher phase noise than the YIG oscillator [2]. The last section is an Automatic Gain Control (AGC) block, a power detector measures the microwave power and the power is adjust through variable gain blocks such as a Variable Gain Amplifier (VGA) or variable attenuators. Figure 4 illustrates a basic block diagram for a signal generator based in a PLL architecture.

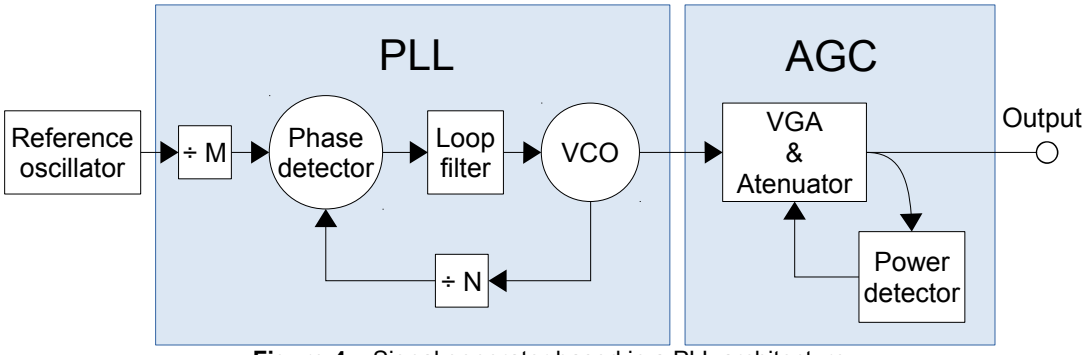


Figure 4 – Signal generator based in a PLL architecture.

Phase noise is expressed in decibels relative to a carrier (dBc), each section of the signal generator have an impact at specific regions of the phase noise spectrum [5]. Figure 5 illustrates the phase noise spectrum of a signal generator based in a PLL architecture, each section of the signal generator has an impact on the phase noise at specific bands.

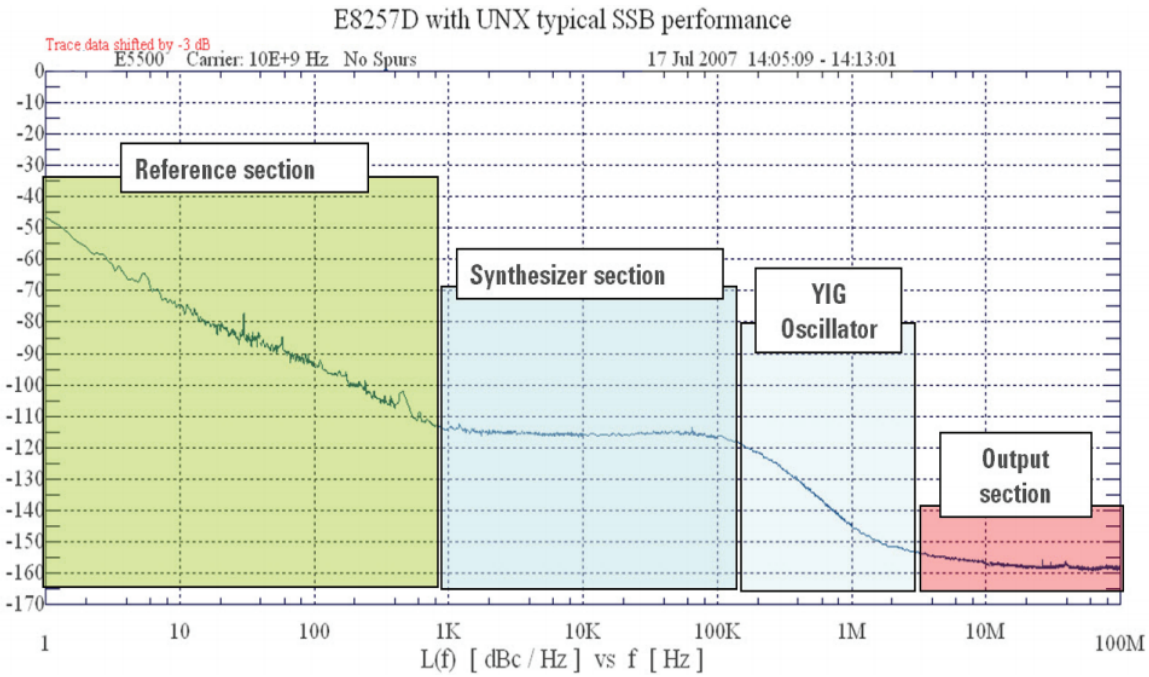


Figure 5 – Phase noise degradation at different bands, credit [5].

As seen in figure 5 the reference section presents a significant phase noise contribution. Keysight uses an integrator as a low pass filter that has the ability to adjust its bandwidth in order to reduce the close-in phase noise [5]. Signal generators can have very complex architectures, per example Keysight has a triple loop architecture that can reduce the phase noise in the pedestal region (offset of 1 kHz to 200 kHz) as much as 12 decibels (dB) [5]. Figure 6 illustrates the mentioned triple loop architecture with an AGC section at the output.

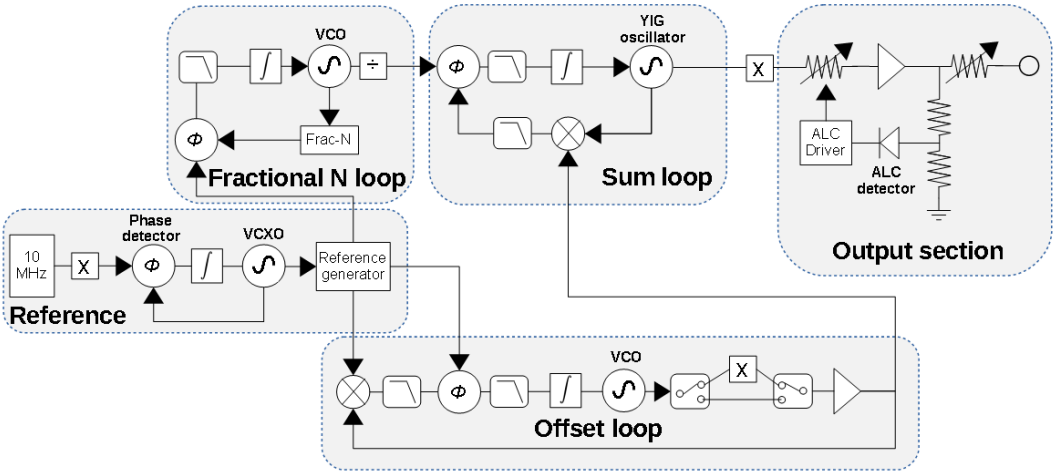


Figure 6 – Keysight triple-loop architecture, adapted from [5].

This type of architectures that uses multiple loops implies a detailed study for each section. It is necessary to alert that this architecture is used in advanced microwave signal generators, although VNAs have similar signal generators.

2.3.2 – Directional coupler - signal coupling

If a transmission line has other lines nearby, the electromagnetic fields will interact meaning that some power is coupled in those lines. In other words, parallel transmission line can act as probes to measure a signal from a main line. VNAs rely on coupling devices, such as directional couplers, in order to acquire a portion of the traveling waves (Incident, transmitted and reflected).

To understand the basics of directional couplers it is necessary to understand the two present modes, even and odd, for the electromagnetic fields between coupled lines. The visualization of the two modes for each field in a cross section of two coupled lines is illustrated in Figure 7.

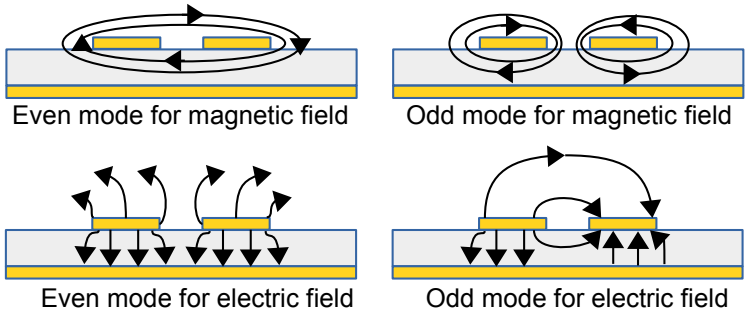


Figure 7 – Even and odd modes for the magnetic and electrical fields in two coupled lines.

For each mode there is a characteristic impedance (Z_O), Z_{Oeven} (characteristic impedance for the even mode) and Z_{Oodd} (characteristic impedance for the odd mode), (4) and (5) allows to calculate the values of Z_{Oeven} and Z_{oodd}.

$$Z_{0even} = Z_0 \sqrt{\frac{1+c}{1-c}} \tag{4}$$

$$Z_{0odd} = Z_0 \sqrt{\frac{1-c}{1+c}} \tag{5}$$

The variable 'c' of (4) and (5) is the coupling in linear units, normally coupling is expressed in dB for that reason 'C' will represent the coupling in dB, (6) gives the 'C'

$$C = 10^{\frac{-c}{20}} \tag{6}$$

Another important relationship when designing coupled lines is between the Z_O, Z_{Oeven} and Z_{Oodd}, which is given by

$$Z_0 = \sqrt{Z_{0even} \times Z_{0odd}} \tag{7}$$

(4) to (7) are fundamental to design a directional coupler. Directional couplers consists on a through path and a coupled path. The coupled path diverts a small amount of the traveling wave of the through path, the amount of the coupled power is determined by the coupling factor.

Figure 8 illustrates the forward coupling factor signals through a directional coupler and an example of the signals power in decibel-milliwatts (dBm).

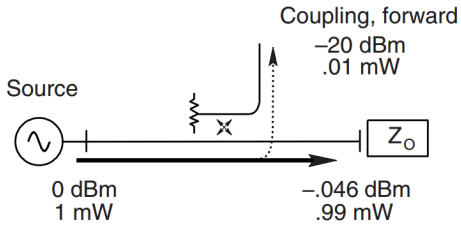


Figure 8 – Forward coupling of a directional coupler, adapted from [4].

The coupling factor in dB is given by

$$C(dB) = -10\text{Log}_{10}\left(\frac{P_{ForwardCoupling}}{P_{Incident}}\right) \tag{8}$$

Another important parameter of a directional coupler is the isolation. Ideally a signal traveling in the opposite direction of the traveling wave should not appear at the coupled port, a way to measure isolation is to send power through the coupler in the opposite direction, and measure the coupled power relative to the incident power [4]. Figure 9 illustrates an isolation example.

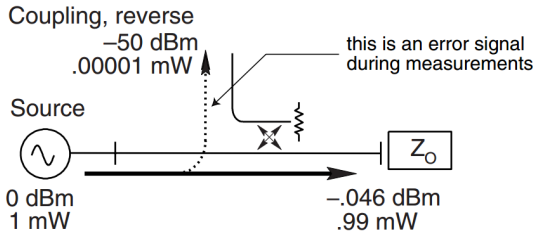


Figure 9 – Isolation of a directional coupler, adapted from [4].

The Isolation Factor in dB for a directional coupler is given by

$$\text{IsolationFactor}(dB) = -10\text{Log}_{10}\left(\frac{P_{ReverseCoupling}}{P_{Incident}}\right) \tag{9}$$

A simple directional coupler has relative narrow bandwidth, it depends on the quarter wavelenght of a specific frequency. Figure 10 shows an 8 GHz bi-directional coupler.

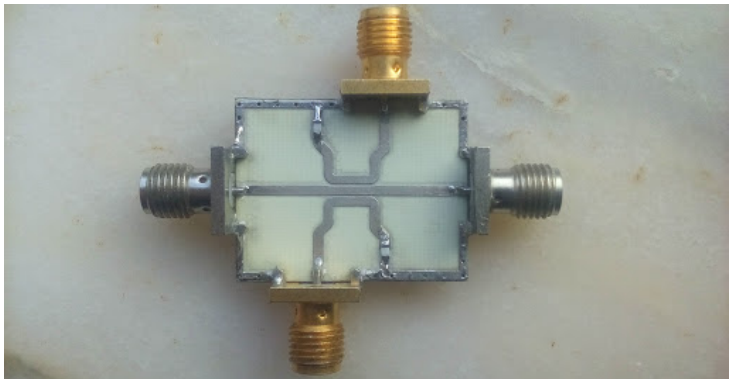


Figure 10 – Bi-directional coupler, single section 8 GHz.

However there are multi-section couplers that can be implemented with striplines on a multi-layer structure achieving bandwidths from 2 GHz to 18 GHz. That type of devices can be used in a VNA for the higher frequency bands but for lower frequencies a modified Wheatstone bridge is the typical solution [6]. An important characteristic of directional couplers is directivity which is the ability to distinguish between the forward signal and the reverse signal, directivity is given by

$$\text{Directivity(dB)} = \text{IsolationFactor} - \text{CouplingFactor} - \text{InsertionLoss} \tag{10}$$

Figure 11 illustrates a microstrip coupler simulation with high directivity between 3,25 GHz to 6 GHz.

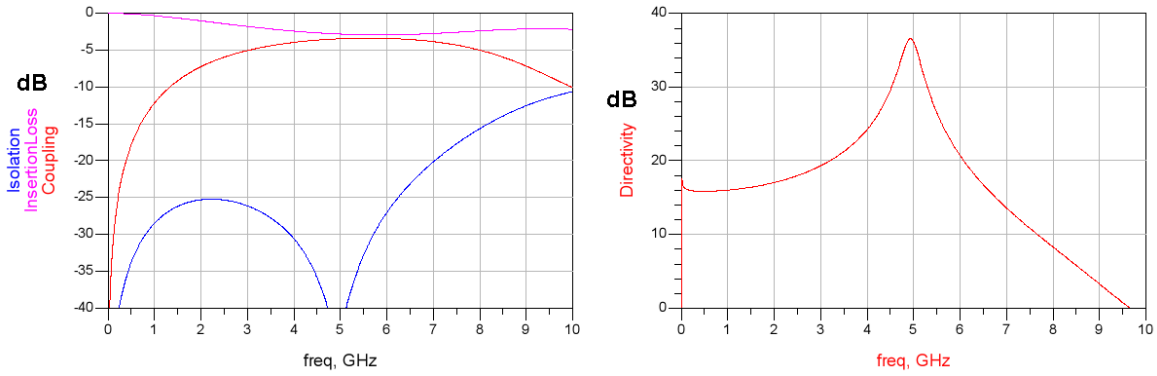


Figure 11 – Microstrip directional coupler simulation.

2.3.3 – Sampling architectures applied to VNAs

To extract the magnitude and phase information VNAs receivers need to down-convert the high frequencies to Intermediate Frequencies (IF), traditional VNA use two types, harmonic samplers and mixer samplers. Each sampler architecture has its advantages and drawbacks: mixers-samplers are often used at RF Frequencies, due to their simplistic architecture that uses a local oscillator and spur management advantage, in the other hand harmonic samplers are used at microwave and millimeter-wave, where receiver compression and cost are critical [7]. Some VNAs have both architectures, such as the MS4640A series from Anritsu [7], in order to optimize performance across the entire frequency range.

Figure 12 shows a generic VNA that uses a Step Recovery Diode (SRD) architecture for sampling.

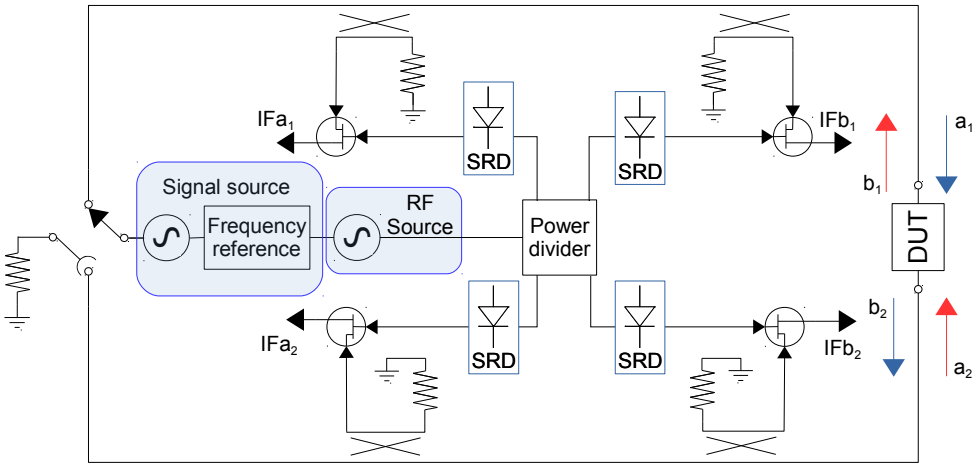


Figure 12 – VNA based on a SRD sampling architecture.

In the harmonic sampler based in a SRD architecture, a SRD is responsible to drive the gate of the sampler. SRDs are popular at microwave engineering because of the ability to rapidly change the junction impedance (low to high). In other words the junction charge is totally removed in a very short period of time creating an abrupt pulse, in the order of pico seconds. This creates significant distortion relative to the input sinusoidal resulting in a comb of harmonics at the output [8]. Figure 13 illustrates an output spectrum of a comb of harmonics.

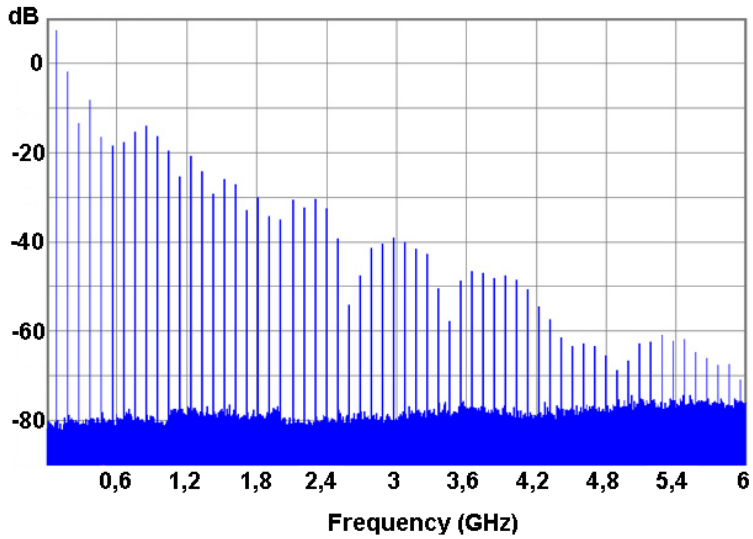


Figure 13 – Comb of harmonics.

In other words SRDs can be used to expand the frequency range, and with proper filtering it is possible to trigger a sampler gate. A sampler block diagram (that could be driven by a SRD) and respective performance for a IF between 100 MHz to 400 MHz using a Metal–semiconductor Field-Effect Transistor (MESFET) is illustrated in Figure 14.

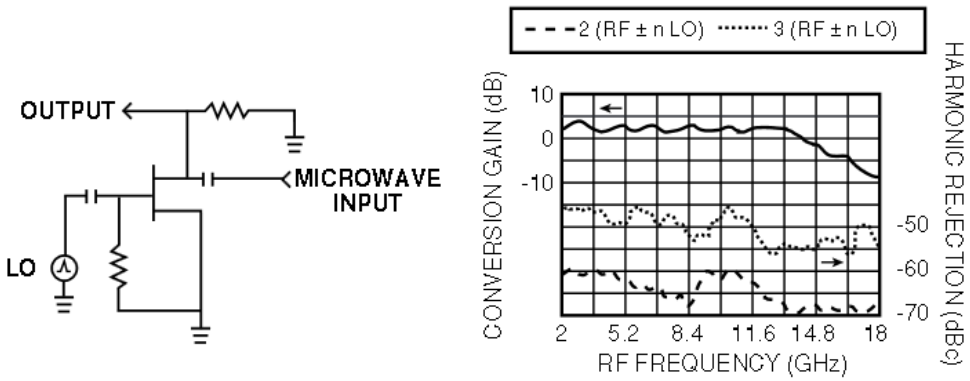


Figure 14 – MESFET sampler from the manufacture Miteq.

It is necessary to take in account that traditional VNAs relied on Schottky diodes as sampler switches [9], but MESFETs have greater isolation properties. Isolation is a difficult problem to solve when SRD are used to drive samplers in VNAs.

For the mixer-sampler approach there are two possible architectures for the tuned receiver, the heterodyne capable to down-convert to IF and the homodyne which makes a direct-conversion called Zero-IF. Figure 15 illustrates the basic architecture of a VNA using mixer-samplers.

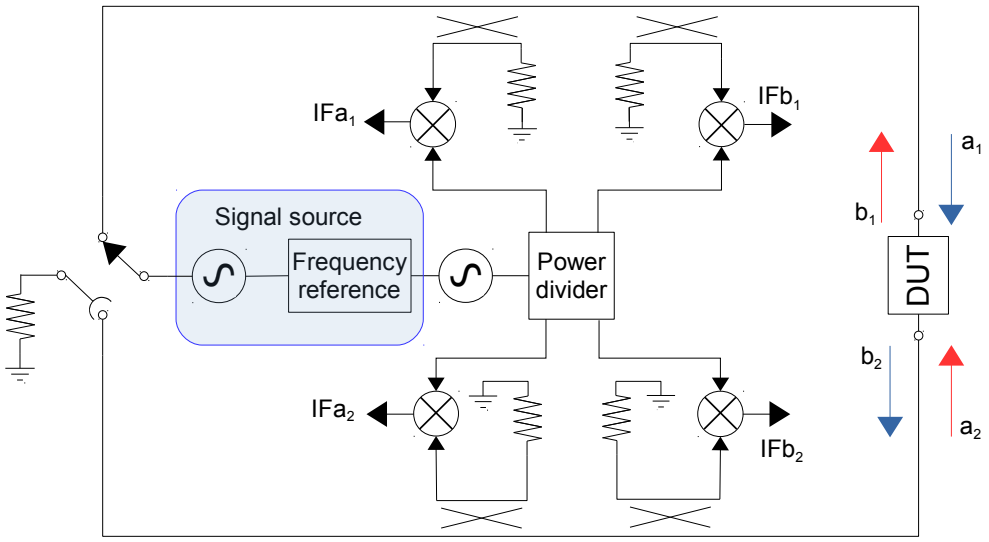


Figure 15 – Block diagram of a VNA using mixers for sampling.

The heterodyne receiver is one of the most used architectures in radio transceivers, it takes advantage of the IF resulted by the multiplication of two sinusoidal signals and the respective filtering. if two sinusoidal signals described by

$$V_{tw} = A_{tw}\mathrm{Cos}(\omega_{tw} t) \tag{11}$$

$$V_{LO} = A_{LO}\mathrm{Cos}(\omega_{LO} t) \tag{12}$$

are multiplied by each other, (11) with (12), results in a new signal:

$$V_x = \frac{A_{LO}A_{tw}}{2}\left[\mathrm{Cos}((\omega_{tw} - \omega_{LO})t) + \mathrm{Cos}((\omega_{tw} + \omega_{LO})t)\right] \tag{13}$$

The formula (13) has two frequencies: one is the sum of ω_{tw} and ω_{LO}, which is called High-IF for up-conversion, the other is the difference between the ω_{tw} and ω_{LO}, named as Low-IF for down-conversion. ADCs in VNA receivers work in undersampling conditions, since the signal is periodic. A generic block diagram for a heterodyne receiver in a VNA is illustrated in figure 16.

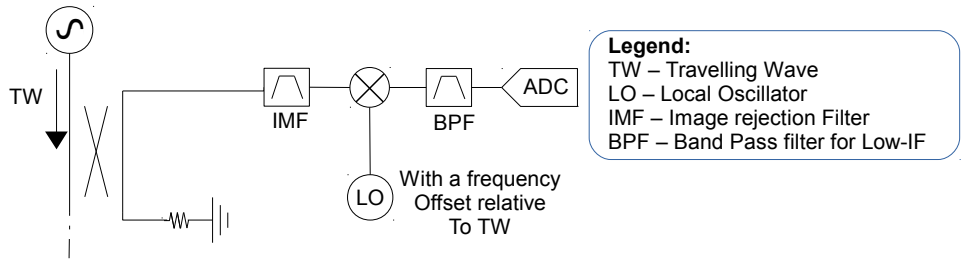


Figure 16 – Heterodyne receiver with a directional coupler.

The homodyne solution is a simplistic architecture, it doesn't need a local oscillator with a frequency offset, it only needs the same frequency with a phase shift. A disadvantage of the homodyne receiver is the DC offsets, since the two input ports have the same frequency it is necessary a higher isolation between them, saturation can also occur if a strong interference enters the two ports of the mixer, self-mixing through the substrate can also ruin the DC value, an illustration of a generic homodyne receiver for a VNA is illustrated in figure 17.

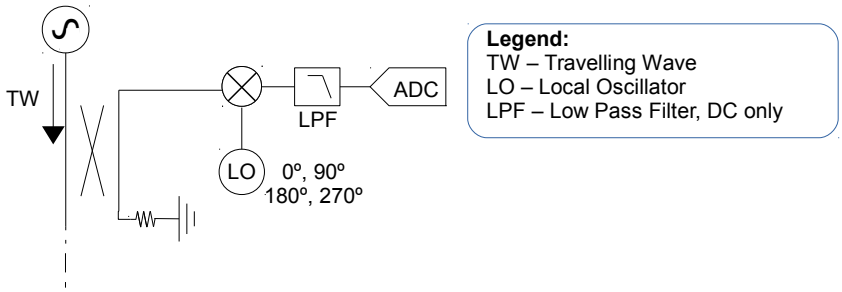


Figure 17 – Basic homodyne receiver with a directional coupler.

To acquire the magnitude and phase measurement, 4 sequential measurements are performed. The local oscillator of the homodyne receiver generates a signal with the same frequency of the traveling wave but with phases offsets of 0º, 90º, 180º and 270º, each measure is then stored and processed in order to calculate, for each frequency, the magnitude and phase given by :

$$A=\frac{1}{2}\sqrt{(U_1-U_3)^2+(U_2-U_4)^2} \tag{14}$$

$$\varphi=\arctan\left(\frac{U_1-U_3}{U_2-U_4}\right) \tag{15}$$

(14) determines the magnitude and (15) the phase as mentioned in [10]. U_1 is the DC value of the

mixer output for a local oscillator with a phase of 0º, U_2 for a 90º offset of the local oscillator, U_3 for a phase of 180º and U_4 for a phase of 270º. This type of architecture takes more time to make a vector measurement at each frequency because of the 4 sequential measurements.

2.3.4 – State-of-the-Art of VNAs

While SRDs allows VNAs to extend their bandwidth up to 65 GHz, they impose a limitation to generate higher harmonic content. However recent implementations of Non-Linear-Transmission-Lines (NLTL) on Gallium Arsenide (GaAs) substrates allows samplers to make down-conversion of millimeter-wave and submillimeter-wave signals possible [7][9].

NLTL is basically a high impedance transmission line loaded, periodically, with hyper abrupt schottky varactors allowing the propagation of nonlinear electrical waves such as shocks and solitons. This type of propagation medium allows to control the phase velocity, as a function of the instantaneous voltage [7][9]. Figure 18 illustrates the output "Shock-Wave" of a NLTL.

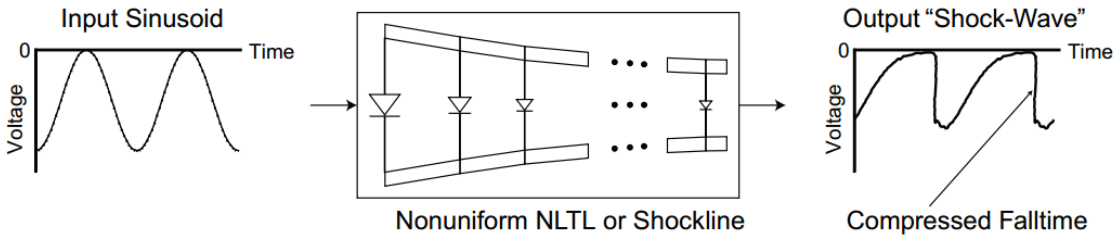


Figure 18 – NLTLs enhance fall time compression [9].

The accentuated fall time of the shock-wave creates a distortion which originates the high content of harmonics to trigger the sampler gates, allowing a significant improvement in sampling architectures. Anritsu exemplifies in [9] the bandwidth improvements between an SRD sampler and a NLTL sampler, illustrated in figure 19.

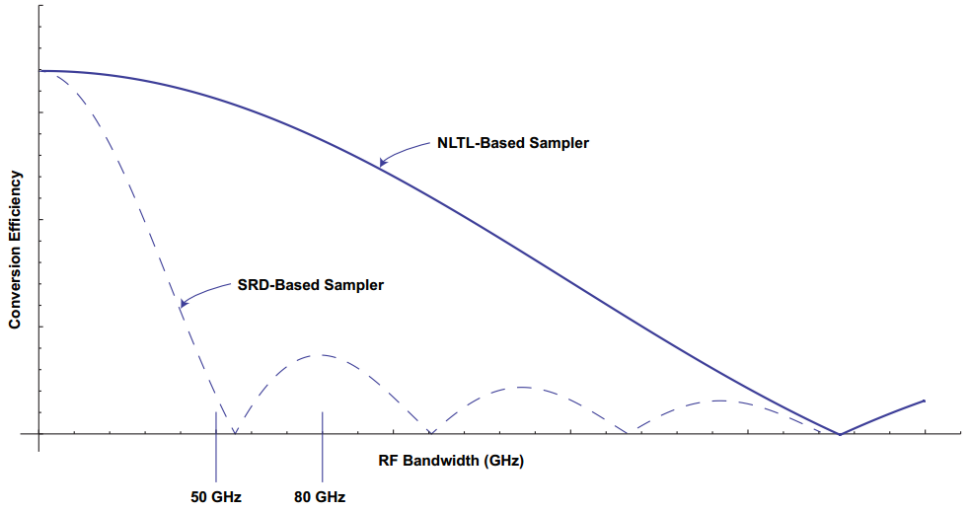


Figure 19 – Conversion efficiency comparison NLTL vs SRD sampler, credit [9].

In patent [11] Anritsu presents a VNA architecture based in NLTL allowing significant improvements in the dynamic range and phase noise. Figure 20 illustrates the dynamic range of a VNA based in NLTL.

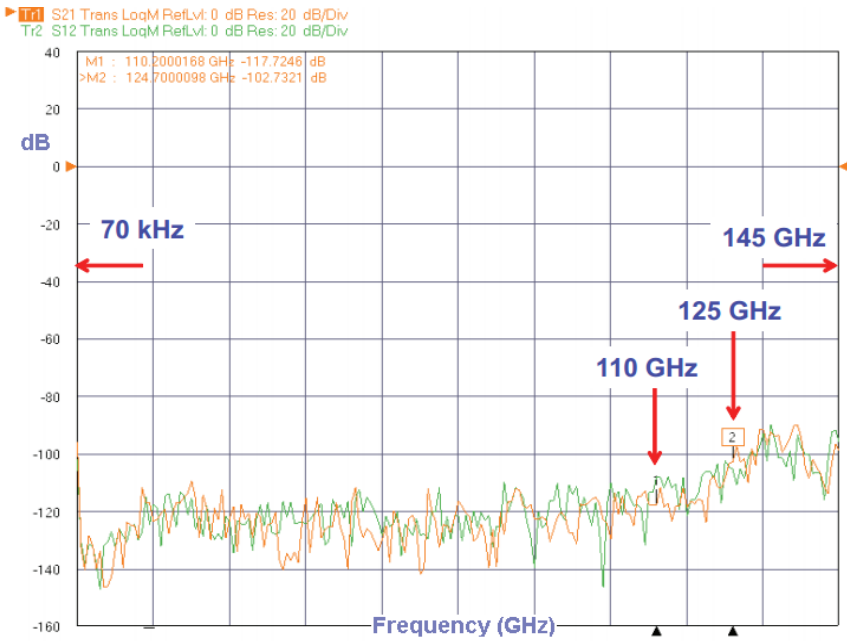


Figure 20 – Measured dynamic range of the NLTL-based VNA, adapted from [5].

The major advantage of Anritsu VNAs based in NLTL technology is high level of monolithic integration, allowing cheaper and compact VNAs. Figure 21 illustrates an integrated reflectometer bridge from Anritsu.

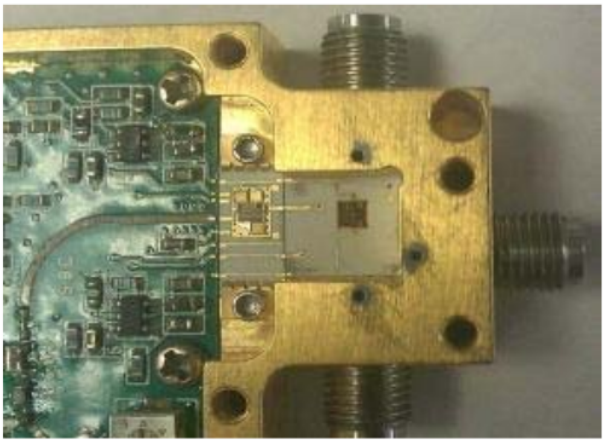


Figure 21 – Anritsu miniature reflectometer, using NLTL technology.

It is necessary to alert that this dissertation doesn't have the objective to use this type of technology. But such information gives the reader the major advantages of VNAs that use NLTL.

Chapter 3 – Transmission lines considerations

3.1 – Comparison between CPWG and microstrip lines

Before addressing the principal circuits that were developed in this work a transmission line study is presented. For such study electromagnetic simulators like the software Advanced Design System (ADS) from Keysight technologies were used.

There are 2 commonly used transmission lines that can be used for this work, microstrip and Co Planar Waveguide With Ground (CPWG). Figure 22 illustrates the transverse section of the microstrip and the CPWG.

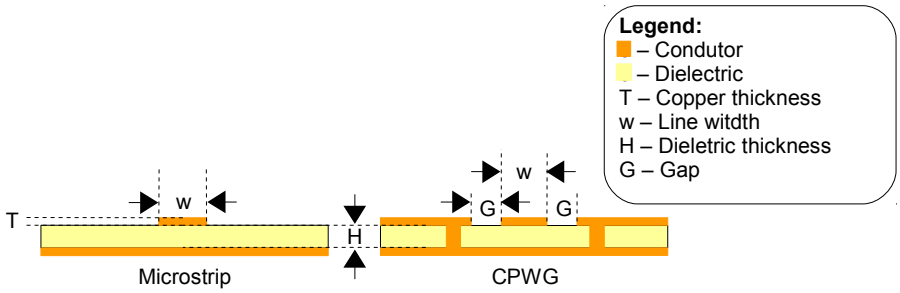


Figure 22 – Transverse section view of a Microstrip and a CPWG.

The microstrip advantage resides in an easier manufacturing process and low insertion losses compared to CPWG with small gaps, the CPWG have the advantage of better electromagnetic confinement resulting in smaller structures which facilitates the Printed Circuit Board (PCB) layout design, in order to minimize Electromagnetic Interference (EMI) or cross talk in other critical sections and have a more stable impedance, a simulation comparison between two CPWG with different gaps and a microstrip was performed, all optimized for a frequency of 24 GHz with a $Z_0 = 50\ \Omega$. Table 3 has the specifications for each line and the substrate specifications.

Table 3 – Specification for the 3 simulated transmission lines (Z_0 = 50 Ω).

Transmission line	CPWG 1	CPWG 2	Microstrip
Line width (w)	0,937171 mm	1,15948 mm	1,12638 mm
Gap (G)	0,3 mm	0,8 mm	doesn't apply
Electrical Length (24 GHz)	900 º	900 º	900 º
Length	20,0512 mm	19,1887 mm	18,514 mm
Substrate: Rogers 4350			
Copper thickness (T)	35 µm		
Dielectric thickness (H)	527 µm		
Loss tangent	0,0035		
Copper roughness	600 nm – Root Mean Square (RMS)		

The results obtained with the ADS software for the 3 transmission lines are illustrated in figure 23.

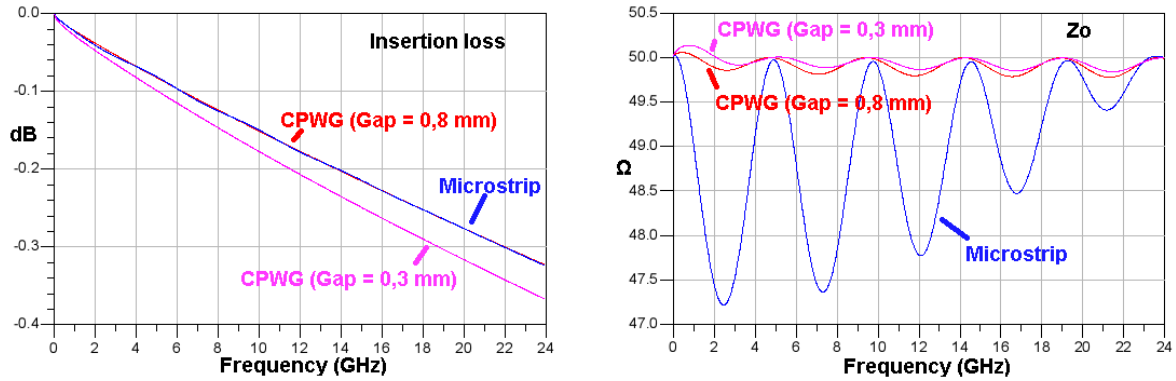


Figure 23 – Comparison performance between transmission lines, simulated in ADS.

As seen in figure 23, the CPWG with a 0,8 mm gap and the microstrip have practically the same insertion loss. However, the microstrip can't maintain a Z_0 = 50 Ω as the CPWG. For such reasons choosing a CPWG is the best solution for covering high bandwidths. Another important aspect is the interface between the transmission line and the connectors, since this work evolved various prototype modules it was necessary to add high performance connectors such as the Sub Miniature version A (SMA) and K (SMK), but this adds a problem, SMA and SMK operate in one mode of interest the Transverse Electromagnetic Mode (TEM) and the CPWG mode is the quasi-TEM and matching the two interfaces can be a problem (a brief study is presented in Section 3.2).

3.2 – CPWG tests with SMA/SMK connectors

Along the work it was necessary to fabricate some transmission lines in order to verify if the manufacturing process allowed high bandwidths with small insertion losses. One test consisted in manufacturing various CPWG with different Gap and measure up to 18 GHz, cut off frequency for the standard SMA. The CPWG were manufactured using the LPKF protomat S62 Computer Numeric Control (CNC) milling machine with a step resolution of 250 nm and with tools that allow a minimum isolation of 200 µm. Figure 24 shows the various lines that were tested with SMAs.

Figure 24 – Various CPWG with different gaps.

The via holes were electroplated and filled with a conductive silver paste, the copper was finished with silver to avoid oxidation. Table 4 has the relevant dimensions of the CPWG lines.

Table 4 – CPWG dimensions for prototyping measurements.

Line Gap (µm)	**Line Width** (mm)		**Substrate Characteristics**	
800	1,1236		Substrate Height	0,527 mm
700	1,1092		ε_r	3,48~3,66
600	1,0887		**Relevant aspects**	
500	1,0600		Vias diameter	0,6 mm
400	1,0150		Space between vias	1,3 mm
300	0,9414		Vias metallization	Electroplating and LPKF ProConduct®
200	0,8136			

The measurement of the lines was performed using the VNA ZVA24 from Rohde & Schwarz, the calibration process used was the Short – Open – Load – Thru (SOLT). Figure 25 shows the insertion loss results.

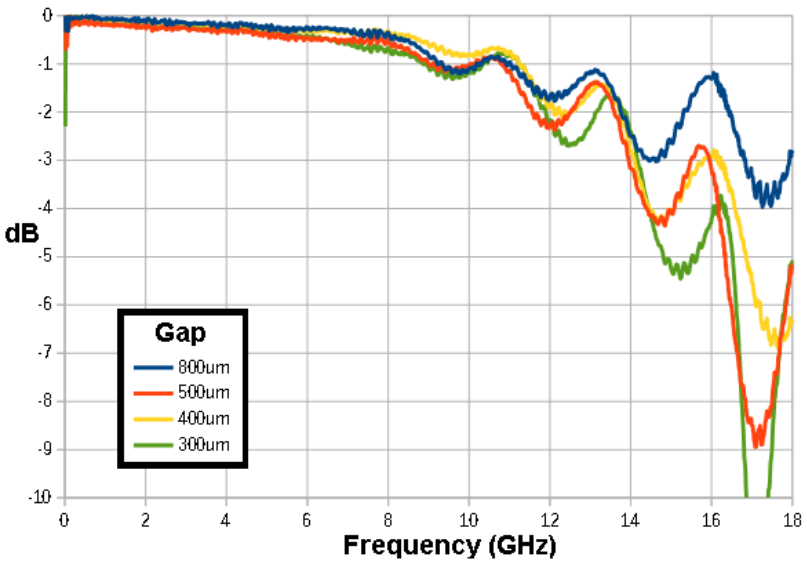


Figure 25 – Prototype CPWG insertion loss measurements with SMA connectores.

The results indicate that a CPWG with 800 µm of gap is the best solution using 3,5 mm SMA connectors. Although is possible to create a smooth transition interface for the electrical and magnetic fields in order to minimize reflections [12][13][14][15]. Figure 26 illustrates a reactive compensation using microstrip sections (this solution it often used for narrow bandwidths).

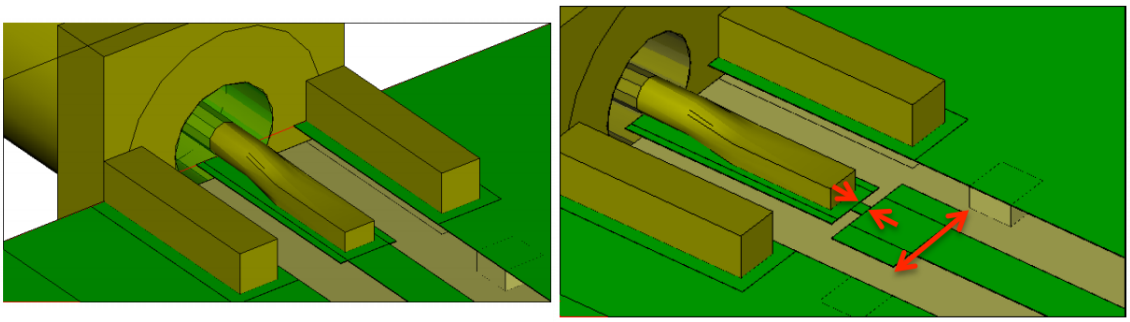


Figure 26 – Reactive compensation using an distributed L-Network, adapted from [14].

But in this work there are some sections that need the full bandwidth, a good solution is provided from microwave companies such as Southwest Microwave that have optimized end launch connectors for the standard substrate thickness. [12][13][15] explains how to optimize transmission lines with end launches using the same substrate of this work and covering important details such as via spacing, Time Domain Reflectometer (TDR) optimization and tapering line optimization from DC to 50 GHz.

Figure 27 shows a 30 mm line mounted on two adjustable brass platforms for prototyping purpose.

Figure 27 – CPWG lenght 30 mm with a 300 um gap, using 2,92 mm SMK connectors.

The major problem of this structure is the air gaps. Some tin between the laminate and the brass structure was added to minimize the air gaps influence. The connectors needed a feed through pin, Figure 28 shows the measurements realized for the line and the 3D electromagnetic simulation results, using the Finite-Difference Time-Domain (FDTD) algorithm. The simulation didn't include the SMK connector but included the feed through pin.

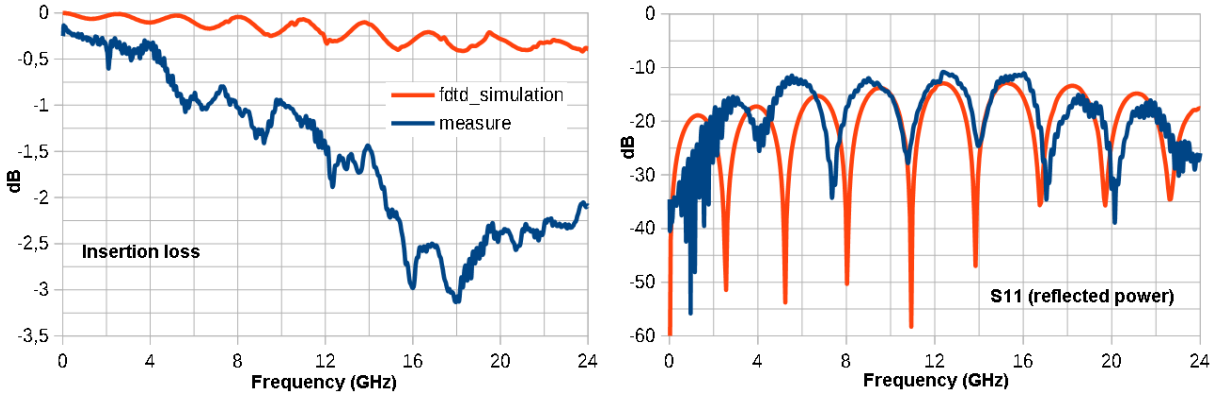


Figure 28 – 30 mm CPWG measured results versus electromagnetic simulation results.

If this solution had a solid construction minimizing air gaps it could be used to prototype the modules of the VNA, however there are some concerns of the vias viability of the CPWG. The substrate is flexible and the metallization of the via can break, causing isolation and bandwidth problems for the CPWG, if the substrate isn't handled with proper care.

Chapter 4 – Signal generator and frequency extension prototypes

4.1 – ADF4351 wide band signal generator prototype

As mentioned in 2.3.1 a signal generator for a VNA should have a low phase noise and a clean frequency tone along its bandwidth. A YIG oscillator is quite expensive or even a wide band VCO such as the HMC733, but Analog Devices ADF435x family offers an alternative solution with low phase noise with competitive prices, Figure 29 shows the phase noise performance of the ADF4351.

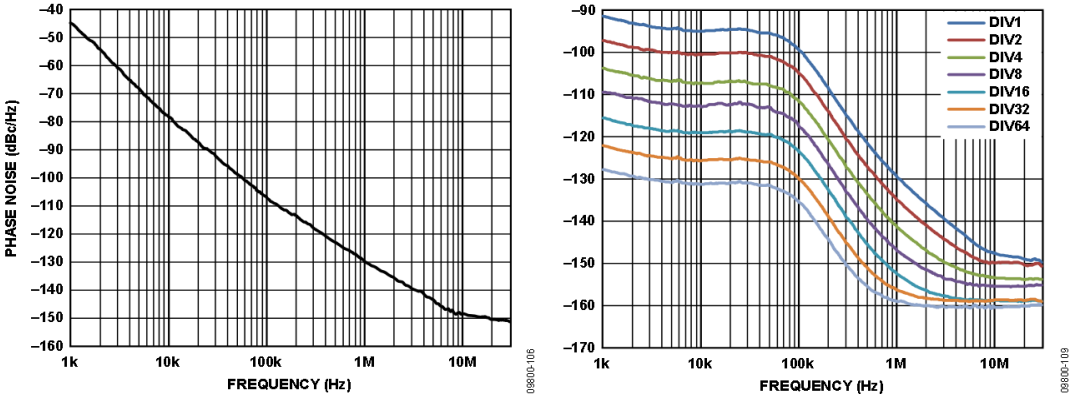


Figure 29 – ADF4351 open-loop VCO phase noise (left), closed-loop for a 4.4 GHz tone (right).

The ADF4351 is a IC integer/fractional synthesizer with a core of three VCO, covering a bandwidth of 35 MHz to 4.4 GHz. With the capability to adjust the output power in 3 dB steps and the phase with a 12 bit word. So it can be used in a homodyne sampler receiver, as mentioned in 2.3.3. The basic architecture for the ADF4351 is illustrated in Figure 30.

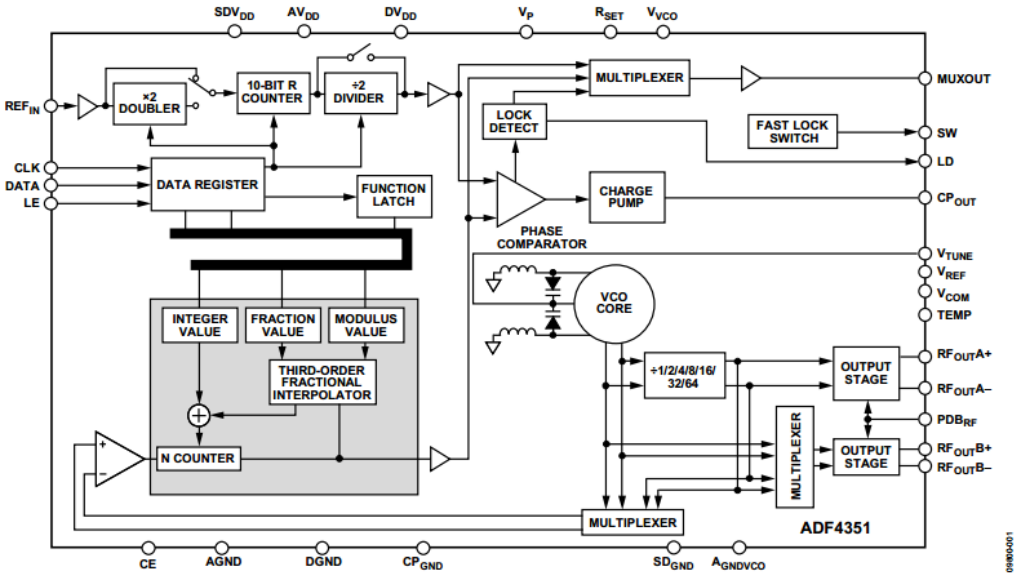


Figure 30 – Functional block diagram for the IC ADF4351.

4.2 – Challenges with the first signal generator prototype ADF4350.

The tests for the IC ADF4351 started on a first prototype board that contains the ADF4350 synthesizer, the major differences between the ADF4350 and the ADF4351 is the output bandwidth and output phase adjustment. The early prototype had a 100 kHz frequency step resolution which is equal to the Phase Frequency Detector (PFD) of the PLL (Appendix 1 and 2 contains the schematics of the ADF4350 signal generator prototype). Figure 31 illustrates the previous signal board prototype board using the ADF4350 with a total bandwidth from 137,5 MHz to 4400 MHz.

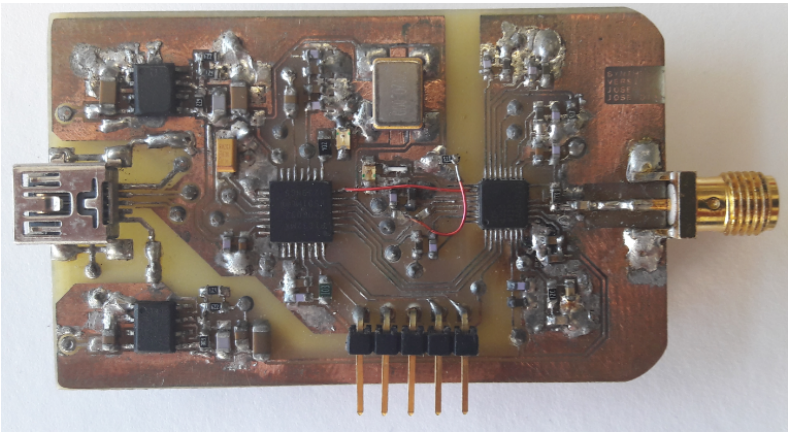


Figure 31 – Previous ADF4350 signal board prototype.

The output power measurements for the early synthesizer board is expressed in Table 5, measured with the Rohde & Schwarz Signal Analyzer FSV 10Hz – 30 GHz.

Table 5 – Output power for the ADF4350 signal generator prototype.

Frequency (MHz)	Output power [dBm]
150	0,81
500	1,07
1000	1,48
1700	2,36
2000	1,55
3000	-1,33
3785	-9,44
4002	-3,53

The values measured for the output power are significantly below the maximum 5 dBm that the IC can deliver, at the time a 50 Ω pull up resistor and a DC block capacitor were used to terminate the open collector of the VCO. This is a very simplistic solution for a broadband bias tee and doesn't provide a good bandwidth match but at the time the major concern was to test the ADF4350 IC. Another aspect is that the board has a layout error, the transmission line should be a 50 Ω CPWG with the dimensions that are illustrated in Table 6.

Table 6 – CPWG characteristics for Z_0 = 50 Ω at 4400 MHz.

Substrate characteristics	ε_R – Dielectric constant	4,6
	Copper conductivity	5,88 x 10^7 S/m
	H – Dielectric height	1,6 mm
	T – Copper thickness	35 µm
	Tangent loss	0,005
CPWG dimensions for a Z_O = 50 Ω at 4400 Mhz	W – Line width	1,04 mm
	G – Gap between the line and the lateral ground	0,2 mm
	Losses in function of length	0,04745 dB/cm

The error created a transmission line with a significant mismatch for a 50 Ω system, and at 4000 MHz, the power drops to -9,44 dBm, as seen in Table 5.

As for the phase noise measurements, a 2000 MHz carrier was tested and it was verified that the noise was significantly high especially at a 10 kHz offset. Table 7 shows the measurements for the ADF4350 signal board prototype.

Table 7 – Phase noise for the ADF4350 signal generator prototype for a 2 GHz carrier.

Frequency offset relative to the carrier	**Phase noise for a 2 GHz carrier** (dBc/Hz)
10 kHz	-52,92
100 kHz	-102,37
200 kHz	-115,06
1 MHz	-128,03

The phase noise could be lower if proper electromagnetic shielding was applied to the whole board. Other aspects that degrades the phase noise are the low PFD, and the oscillator reference noise, in this case a 20 MHz with a stability of ± 25 Parts Per Million (PPM) meaning a 20 MHz oscillator with a frequency deviation of ±500 Hz.

Although the board had some problems, especially in delivering the 5 dBm, it was able to lock to the desired frequency. Figure 32 illustrates the PLL locked at the minimum frequency 137,5 MHz with the measurement made using the Keysight N9320B RF Spectrum Analyzer 9 kHz to 3.0 GHz.

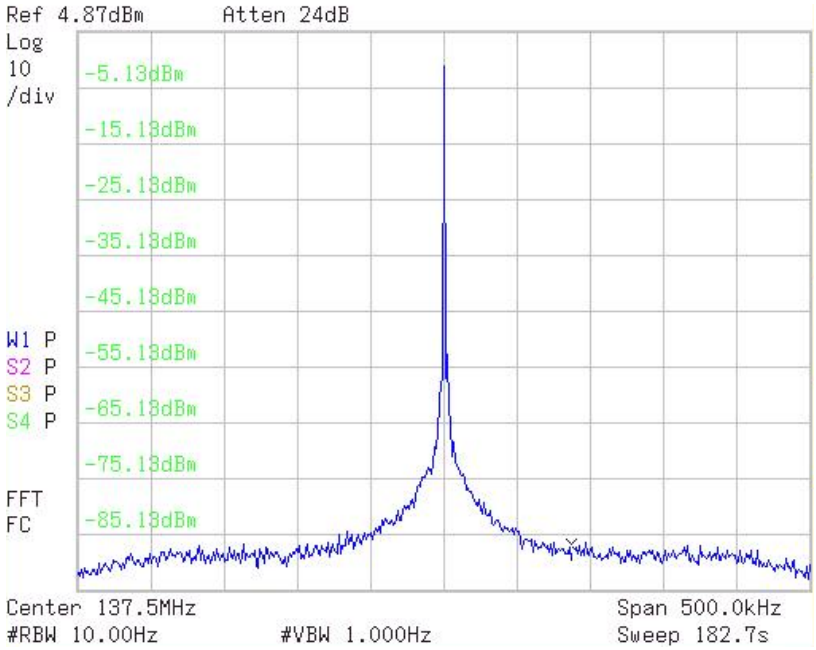


Figure 32 – Output spectrum for the ADF4350 signal board at 137,5 MHz.

In order to solve the problem of the output power and the phase noise performance below a 10 kHz carrier offset, a different approach had to be taken, which was to separate the signal generator in modules and to create a section for changing the filter of the charge pump that drives the oscillator core. Other sections were also external such as power supply and the microcontroler board.

4.3 – ADF4351 signal generator board design

With the aid of the software ADIsimPLL a loop filter was dimensioned, the filter is responsible to clear the spurious of the output of the charge pump, pin CP_{out}, in order to drive the VCO core through the pin V_{TUNE}. The values were calculated for a loop bandwidth of 25,2 kHz and a phase margin of 45º, so the filter components values are presented in Figure 33.

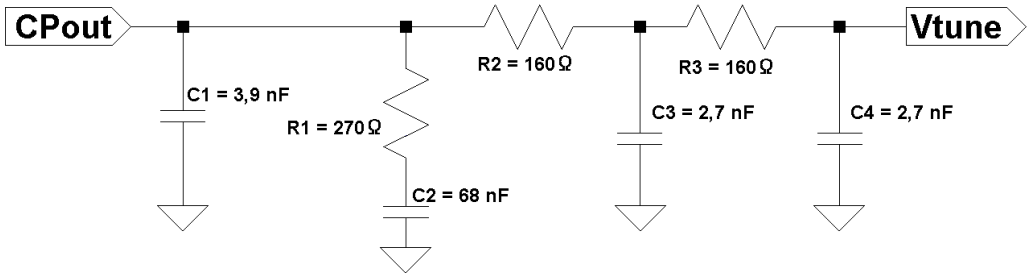


Figure 33 – Filter for the PLL, with a loop bandwidth of 25,2 kHz with a 45º of phase margin.

In order to minimize the synthesizer phase noise, the frequency of comparison of the phase detector was maximized to 10 MHz. The synthesizer was set to work only in integer mode, as mentioned in [16], which is significant disadvantage in frequency step resolution. Using the PLL in fractional mode creates significant spurious because of the 3rd order fractional interpolater. Another aspect is related with the relation between the higher PFD and the loop bandwidth of 25,2 kHz, for the first prototype using the IC ADF4350, the loop bandwidth was 9,78 kHz with a PFD of 100 kHz this allows a faster filter response for the adjustments of the phase detector, but the phase noise is higher.

There is a solution for lower frequency step, a Direct Digital Synthesizer (DDS) can be used as a signal reference for the PLL, per example IC AD9951 has a 32-bit frequency tuning word capable to achieve a frequency resolution of 100 mHz, and a residual phase noise of -120 dBC/Hz at a 10 Hz offset relative to a 9,5 MHz carrier. Unfortunately with the complexity and unexpected problems along the work it wasn't possible to implement this solution, however an external input for future tests was included. Figure 34 shows a photo of ADF4351 signal board prototype.

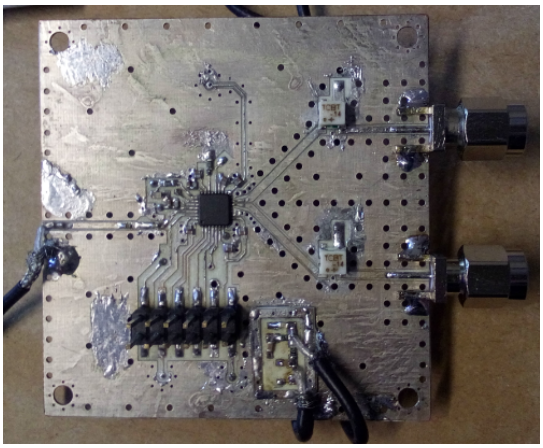


Figure 34 – ADF4351 signal generator prototype.

The output section of the ADF4351 is a differential open collector and there is the necessity to add external bias. For that purpose a mini circuits TCBT-14+ wide band bias tee was applied in order to polarize the differential pair and isolate the linear regulators from receiving unwanted RF signal, Figure 35 shows the output stage of the ADF4351.

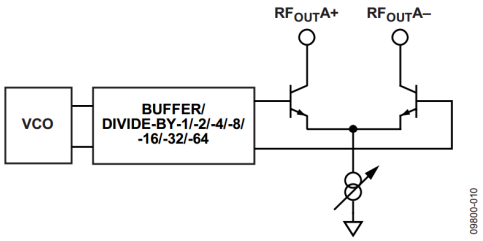


Figure 35 – ADF4351 RF output stage.

The transmission line that was applied in the board is a CPWG designed on the Rogers4350 substrate, the output connectors are the standard SMA plugs. Table 8 indicates the dimensions of the CPWG.

Table 8 – CPWG dimensions for the output section of the ADF4351.

Design frequency (MHz)	4400	$\mathbf{Z_0}$ (Ω)	50
Width (mm)	0,93	**Length** (mm)	22,92
Gap (µm)	300	**Electrical Length** (Degrees)	180
Substrate Height (µm)	525,78	**Relative Permittivity**	3,48
Copper Height (µm)	35	**Via holes diameter** (mm)	1

4.4 – ADF4351 signal generator control software

Since the number of control variables for the ADF435x family is considerable, a Graphic User Interface (GUI) was made in Microsoft visual studio c++ for the Operating System (OS) Windows 7, in order to aid the development of the basic firmware to control the IC ADF4351. The microcontroler responsible to configure the PLL synthesizer is the PIC32MX220FB, it has a Serial Peripheral interface (SPI) BUS for writing the synthesizer registers and a Universal Serial Bus (USB) to communicate and several re-mappable IO ports. Figure 36 illustrates the developed GUI for debugging purposes.

Figure 36 – GUI software for the ADF4351 signal generator prototype.

The software isn't complete, the sweep time is fixed, but allows to configure the 5 registers of the ADF4351 and to set the desired frequency from 35 MHz to 4400 MHz and allows frequency sweeps. The frequency step resolution can also be changed in order to test the impact on the PLL, especially on the loop filter for cleaning the spurious of the charge pump derived from the phase comparator.

4.5 – ADF4351 signal generator measurements

The measured results for the signal generator using the ADF4351 were measured with the R&S® FSV Signal and Spectrum Analyzer. Table 9 shows the measured results for the output power of the fundamental frequency and the unwanted harmonics.

Table 9 – ADF4351 basic signal generator power measurements.

Frequency (MHz)	**Fundamental** (dBm)	**2nd harmonic rejection** (dBc)	**3rd harmonic rejection** (dBc)
2000	5,11	26,53	15,1
2200	5,48	26,36	
3000	3,81	15,89	18,24
4000	2,96	32,51	25,48
4400	3,52	24,23	32,69

The output power has been significantly improved in the band of 2 GHz to 4,4 GHz. Since the maximum power of the ADF4351 is 5 dBm, the power problem is solved. The 2nd and 3rd harmonics are significantly high which was expected since there is no filtering. The phase noise could not be measured at PFD of 10 MHz because the PLL sometimes losses the lock. Further tuning test will be needed in order to correct the problem that doesn't always occur.

4.6 – Frequency extension prototype modules

To extend the frequency bandwidth of the ADF4351 signal generator board a market component identification was made. It was very difficult to find frequency multipliers for extending the bandwidth of the ADF4351. However, it was possible to find two passive diode balun doublers, the HMC189 with an output frequency from 4 GHz to 8 GHz and the HMC204 which extends from 8 GHz to 16 GHz. For the last frequency multiplication stage the AMMP-6120 active doubler was included allowing to extend the bandwidth from 16 GHz to 24 GHz with odd harmonic cancellation. Figure 37 illustrates the architectures of the HMC189, HMC204 and the AMMP-6120.

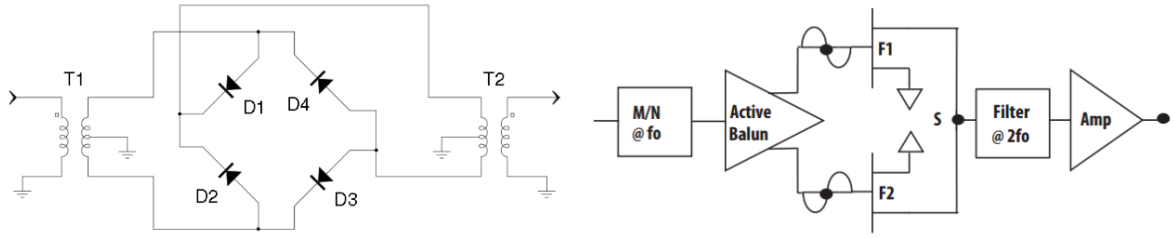


Figure 37 – HMC189/204 architecture (left) and the AMMP 6120 (right).

The two passive diode balun doublers have a significant high conversion loss (around 15 dB) and need at least 15 dBm of input power in order to present those conversion losses in the pretended band. Taking in consideration this aspect a first architecture was set in order to study the complete circuit. Figure 38 illustrates the first architecture proposed for the frequency extender.

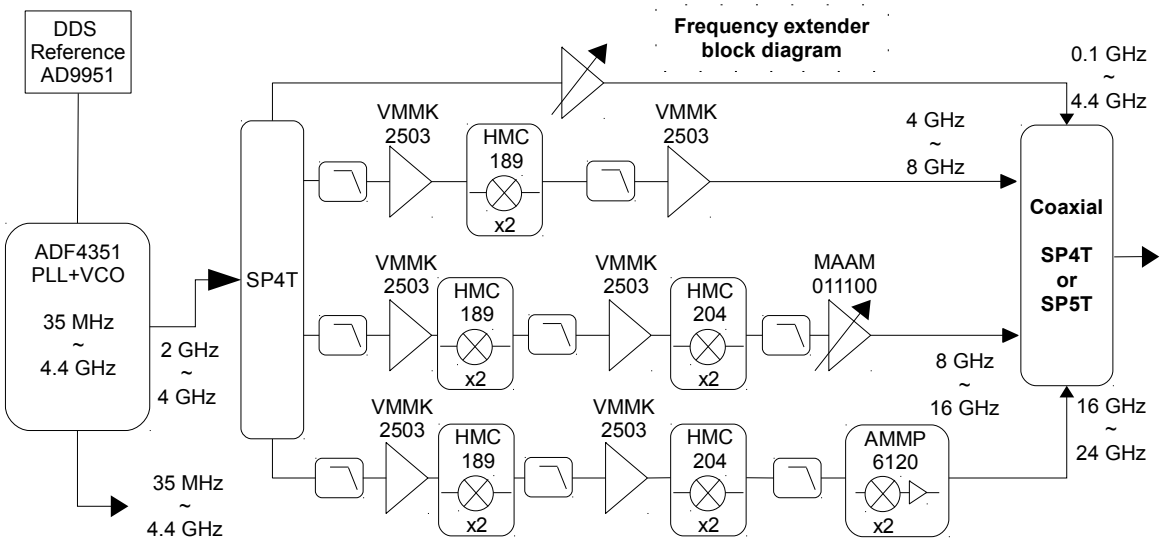


Figure 38 – First frequency extender block diagram and ADF4351 signal generator.

As seen in Figure 38, the amplifier VMMK 2503 was included at the input of the two passive doublers in order to drive them. When this architecture was proposed the major concern was the intermodulation products which could inflict significant harmonic distortion. The manufacture of the passive doublers doesn't specify the conversion losses for higher and lower frequencies, meaning that it is necessary to characterize. It is also necessary to filter the input of all doublers in order to minimize the presence of the unwanted harmonics, per example if the doubler HMC189 has an input bandwidth of 2 GHz to 4 GHz it would be necessary to filter above 4 GHz but when an input stimulus of 2 GHz is applied the filter won't attenuate the 2^{nd} harmonic. So intermodulation problems could appear at the end of the last multiplier and it would be required a significant number of filters and a multiplexing section, which will increase insertion losses leading to a new architecture.

Tests were made in order to measure the power level of the harmonics and to measure if the output power of each multiplication section is sufficient for driving the next one. Table 10 shows the characteristics of the passive doublers and amplifiers for extend the bandwidth up to 16 GHz.

Table 10 – Characteristics of the key components for the frequency extender modules.

HMC189 conversion loss (dB)	VMMK-2503 gain (dB)	HMC204 conversion loss (dB)	MAAM 011100 minimum gain (dB)	MAAM 011100 maximum gain (dB)
-12 (4 GHz)	14,2 (4 GHz)	-17,5 (8 GHz)	-20 (8 GHz)	10 (8 GHz)
-11,5 (6 GHz)	13,8 (6 GHz)	-16 (12 GHz)	-20 (12 GHz)	10 (12 GHz)
-14 (8 GHz)	13,23 (8 GHz)	-18 (16 GHz)	-20 (16 GHz)	10 (16 GHz)

The tests were performed in 4 prototype modules, that were considered important for this architecture: Module A, with an amplified output 4 GHz to 8 GHz bandwidth; Module B1 without output amplification with an output bandwidth from 8 GHz to 16 GHz; Module B2 with output amplification and an output bandwidth of 8 GHz to 16 GHz and a fourth module capable to extend the bandwidth up to 24 GHz.

4.6.1 – Module A – 4 GHz to 8 GHz measurements

Module A that is composed by the passive GaAs bridge doubler HMC189 and the amplifier VMMK-2503, covers the band 4 GHz to 8 GHz. The bias tee components were carefully chosen in order to choke the RF signal to minimize the presence in the DC path. The block diagram of the first frequency extension module is illustrated in Figure 39.

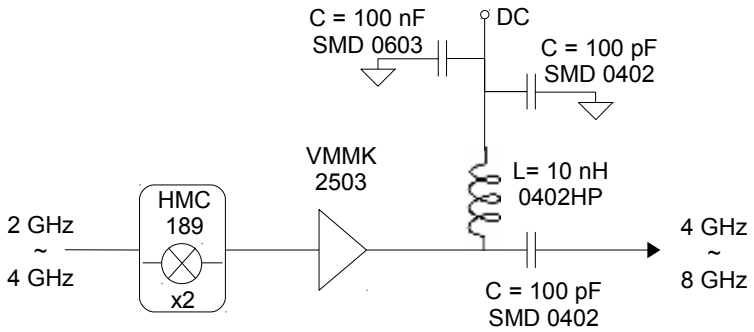
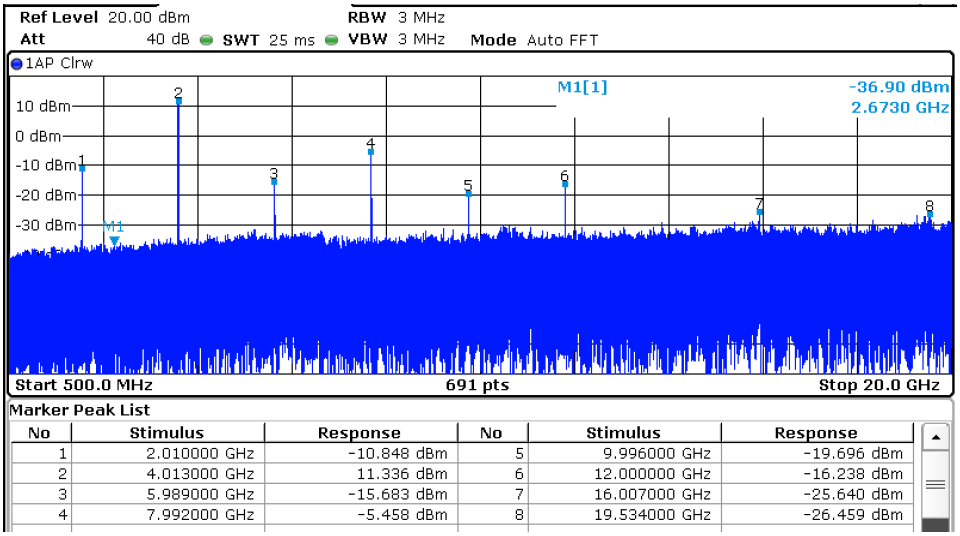


Figure 39 – Frequency extension block diagram for Module A, 4 GHz to 8 GHz.

The doubler HMC189 needs at least 15 dBm in order to produce an output without significant unwanted harmonics, a 20 dB harmonic rejection should be enough for a prototype without any filtering section. Measurements were conducted for a 15 dBm input stimulus for the input band 2 GHz to 4 GHz, Figure 40 illustrates the output spectrum for a 2 GHz input stimulus applied to the Module A.



No	Stimulus	Response	No	Stimulus	Response
1	2.010000 GHz	-10.848 dBm	5	9.996000 GHz	-19.696 dBm
2	4.013000 GHz	11.336 dBm	6	12.000000 GHz	-16.238 dBm
3	5.989000 GHz	-15.683 dBm	7	16.007000 GHz	-25.640 dBm
4	7.992000 GHz	-5.458 dBm	8	19.534000 GHz	-26.459 dBm

Figure 40 – Output spectrum of Module A, 15 dBm input signal 2 GHz.

The harmonic rejection for an output frequency of 4 GHz is 16,8 dB, but this value can be improved in the layout of the PCB creating a wall of via fences [17]. Another important aspect are the connectors, they weren't DE-Embedded. It is necessary to alert that the following results only give an idea of the power level of the unwanted harmonics, the resolution filter and the video filter of the spectrum analyzer have high bandwidths, when it should be low (it is recommended to repeat the measurements in order to make accurate measurements). However it is possible to identify the power of the significant harmonics. The next step was to measure for a 3 GHz input frequency, the results were practically the same as for the 2 GHz input, as Figure 41 shows.

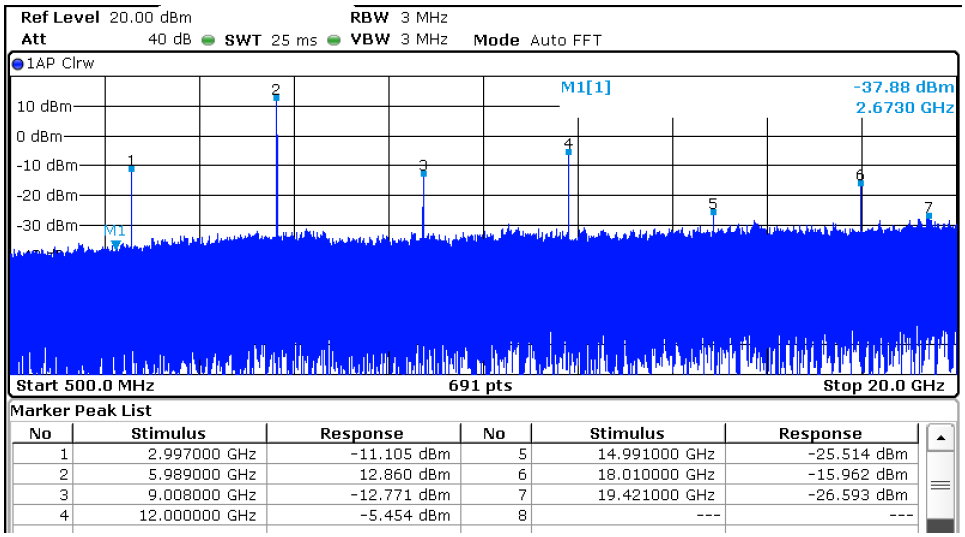


Figure 41 – Output spectrum of the Module A, input signal 3 GHz.

For a 4 GHz input stimulus the unwanted harmonics are 17 dB below the 8 GHz output, as it can be see in Figure 42.

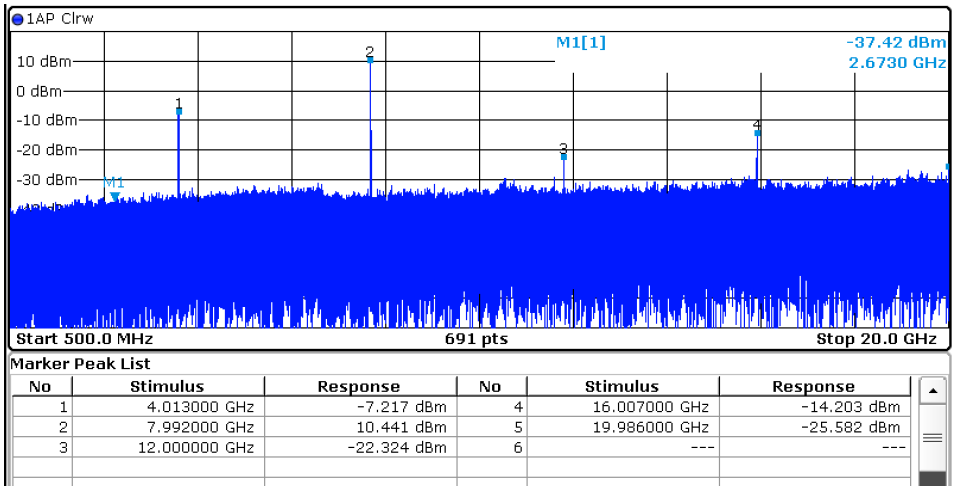


Figure 42 – Output spectrum of the Module A, input signal 4 GHz.

The results for the first prototype module clearly can cover the 4 GHz to 8 GHz band, nevertheless the 13 dBm output power may be insufficient to drive the next stage (15 dBm), but it is necessary to take in account that the connectors influence weren't DE-embedded and the line length wasn't optimized at the time.

4.6.2 – Module B1 and B2 – 8 GHz to 16 GHz measurements

In order to evaluate the multiplier extension stage, two prototypes were developed. One was to measure if the doubler HMC204, without amplification, was capable to drive the active doubler, AMMP-6120, for the last multiplication stage (input frequency 8 GHz to 12GHz) and the other was simply to cover the 8 GHz to 16 GHz band with amplification.

4.6.2.1 – Module B1 – 8 GHz to 16 GHz without output amplification

The following block diagram of Figure 43 shows the prototype for the measurements of the bandwidth 8 GHz to 16 GHz without output amplification.

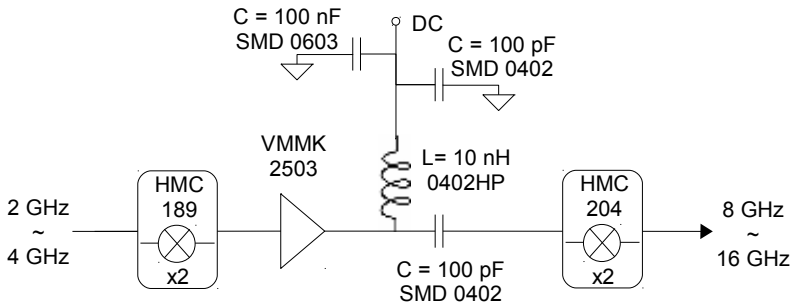
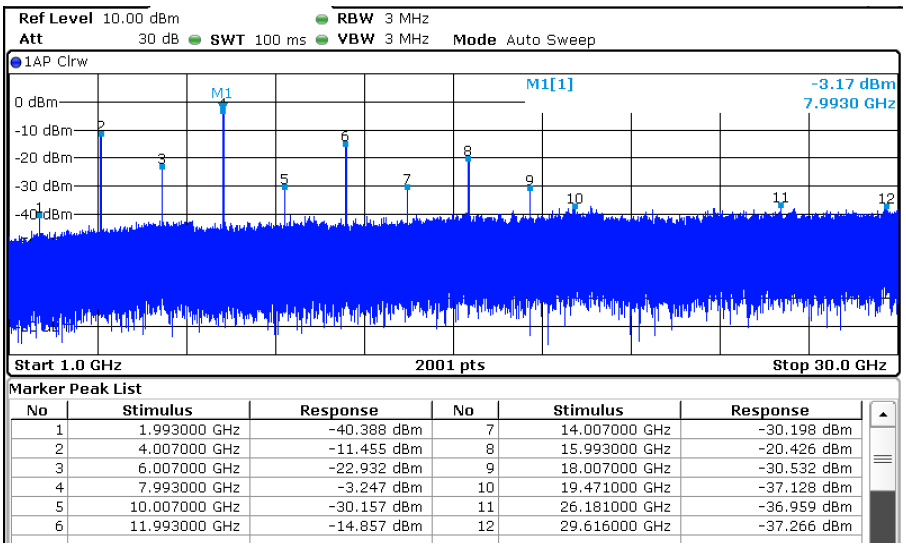


Figure 43 – Frequency extension block diagram for Module B1, 8 GHz to 16 GHz.

Figure 44 shows the desired 8 GHz fundamental for a 2 GHz input frequency and unwanted harmonics.



No	Stimulus	Response	No	Stimulus	Response
1	1.993000 GHz	-40.388 dBm	7	14.007000 GHz	-30.198 dBm
2	4.007000 GHz	-11.455 dBm	8	15.993000 GHz	-20.426 dBm
3	6.007000 GHz	-22.932 dBm	9	18.007000 GHz	-30.532 dBm
4	7.993000 GHz	-3.247 dBm	10	19.471000 GHz	-37.128 dBm
5	10.007000 GHz	-30.157 dBm	11	26.181000 GHz	-36.959 dBm
6	11.993000 GHz	-14.857 dBm	12	29.616000 GHz	-37.266 dBm

Figure 44 – Frequency extension block diagram for Module B1, input signal 2 GHz.

Compared to the previous frequency multiplier, Module A, the CPWG is significantly different, the gap between the ground and the feed line is superior. Figure 45 illustrates the difference between the two modules A and B1.

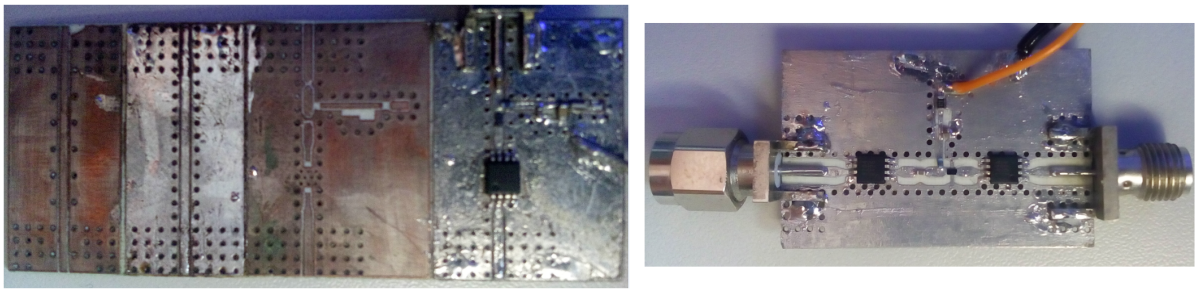
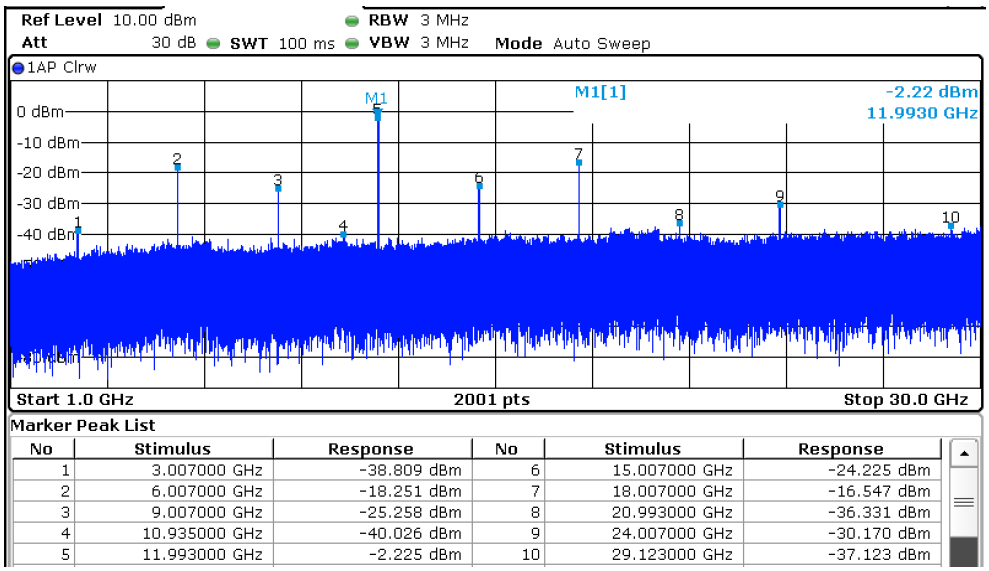


Figure 45 – Module A: 4 GHz to 8 GHz (left), Module B1: 8 GHz to 16 GHz (right).

The reason to try to change the gap was to minimize the manufacturing error, and to minimize reflections from mismatches, as mentioned in section 3.1. For testing the 12 GHz output power level a 3 GHz input frequency was applied in Module B1. Figure 46 shows the output spectrum from a 3 GHz input stimulus.



No	Stimulus	Response	No	Stimulus	Response
1	3.007000 GHz	-38.809 dBm	6	15.007000 GHz	-24.225 dBm
2	6.007000 GHz	-18.251 dBm	7	18.007000 GHz	-16.547 dBm
3	9.007000 GHz	-25.258 dBm	8	20.993000 GHz	-36.331 dBm
4	10.935000 GHz	-40.026 dBm	9	24.007000 GHz	-30.170 dBm
5	11.993000 GHz	-2.225 dBm	10	29.123000 GHz	-37.123 dBm

Figure 46 – Frequency extension block diagram for Module B1, input signal 3 GHz.

The measurements indicates that there is sufficient power for the 8 GHz to 12 GHz band for driving the next active frequency doubler, AMMP-6120, using SMA connectors. However, there is some concerns relative to the unwanted harmonics and amplifier saturation. Per example, at 16 GHz the output power drops significantly compared to the unwanted harmonics and filtering in such conditions can be difficult. Figure 47 illustrates the output spectrum of Module B1 for a 4 GHz input frequency.

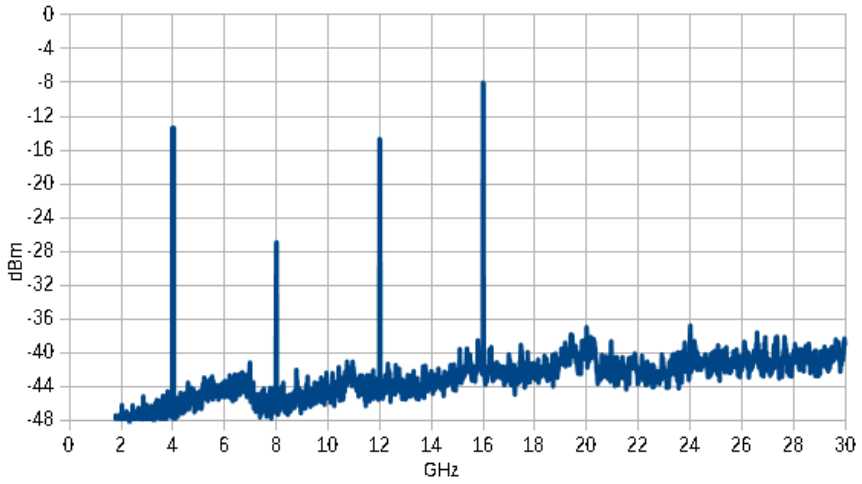


Figure 47 – Frequency extension block diagram for Module B1, input signal 4 GHz.

4.6.2.2 – Module B2 - 8 GHz to 16 GHz with output amplification

With the results obtained with Module B1, 8 GHz to 16 GHz without amplification, it was necessary to find an amplifier in order to amplify the referred band. For this module the first frequency multiplier wasn't included in order to have a similar comparison with module A. Figure 48 illustrates the block diagram for the Module B2.

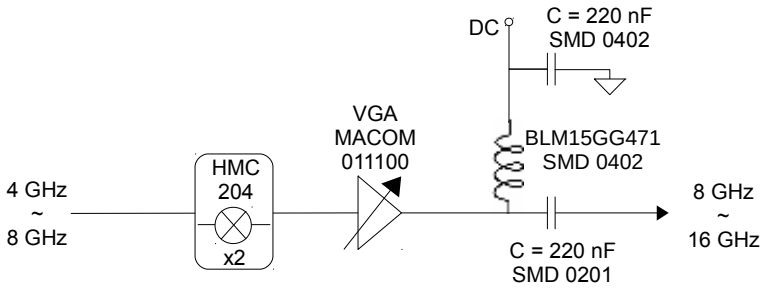
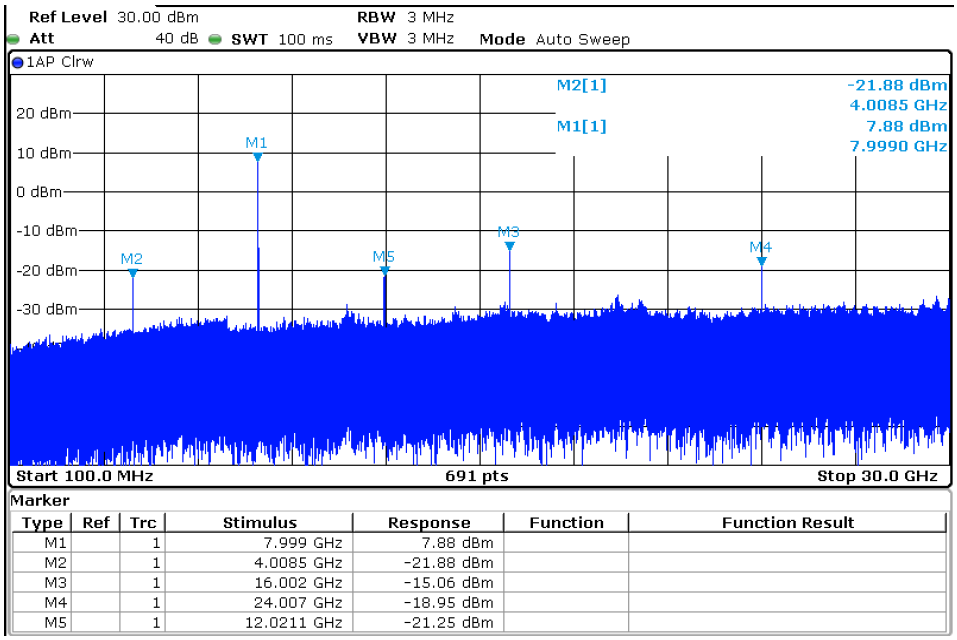


Figure 48 – Module B2 – 8 GHz to 16 GHz.

The results obtain for a 4 GHz input that results in an 8 GHz output fundamental is illustrated in Figure 49.



Marker

Type	Ref	Trc	Stimulus	Response	Function	Function Result
M1		1	7.999 GHz	7.88 dBm		
M2		1	4.0085 GHz	-21.88 dBm		
M3		1	16.002 GHz	-15.06 dBm		
M4		1	24.007 GHz	-18.95 dBm		
M5		1	12.0211 GHz	-21.25 dBm		

Figure 49 – Frequency extension block diagram for Module B2, input signal 4 GHz.

The output frequency spectrum for an input frequency of 6 GHz, which will give a 12 GHz harmonic output, Figure 50 shows the measurement for module B2 with an input signal of 6 GHz.

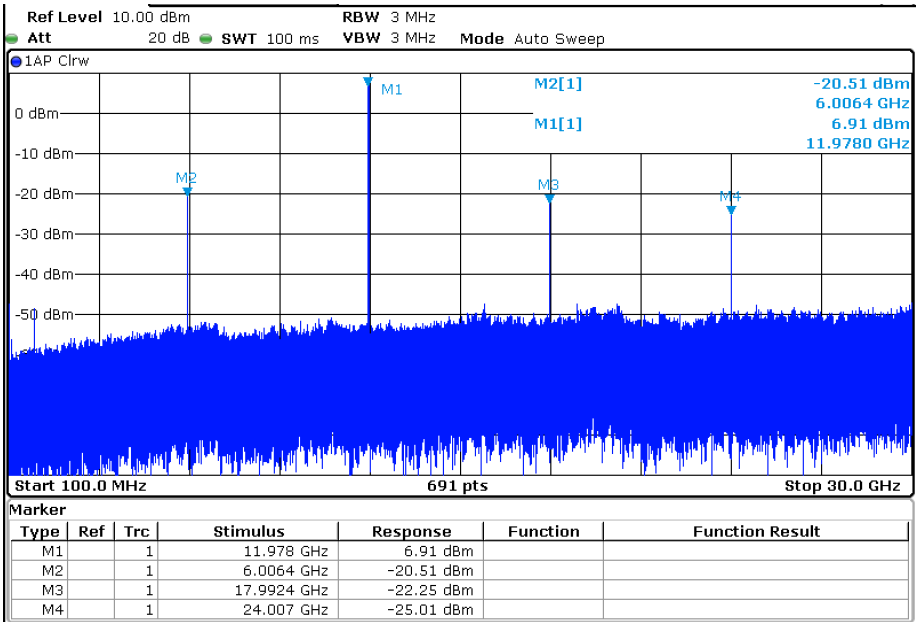


Figure 50 – Frequency extension block diagram for Module B2, input signal 6 GHz.

And the last one for an 8 GHz input frequency which gives a 16 GHz output is illustrated in Figure 51.

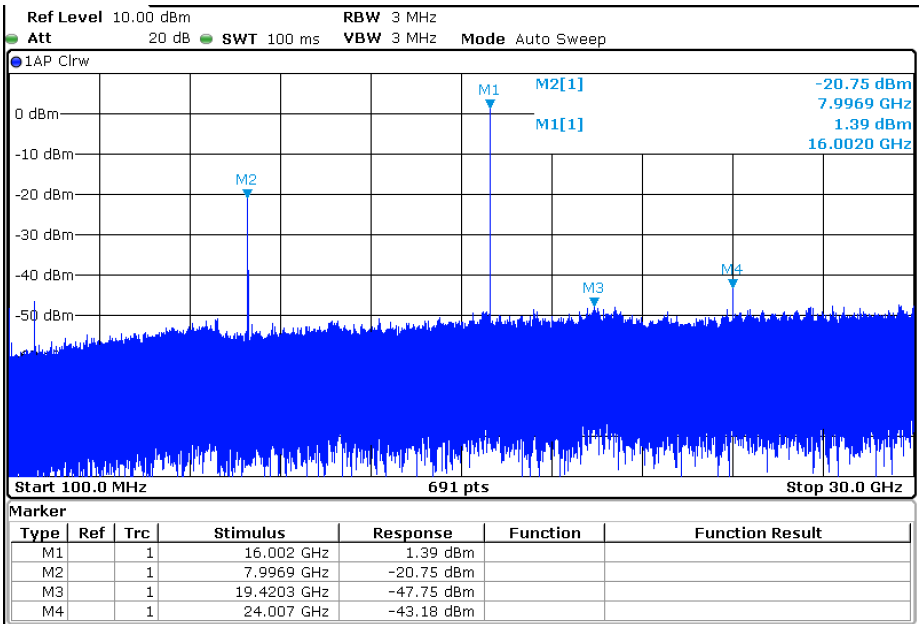


Figure 51 – Frequency extension block diagram for Module B2, input signal 8 GHz.

The harmonic rejection for the module B2 is 22 dB, such value is still high, but a filtering section should minimize the harmonic content. There was an improvement that minimizes the presence of the input frequency signal at the output. A wall of via fences was introduced as can be seen in Figure 52 that shows the test Module B2.

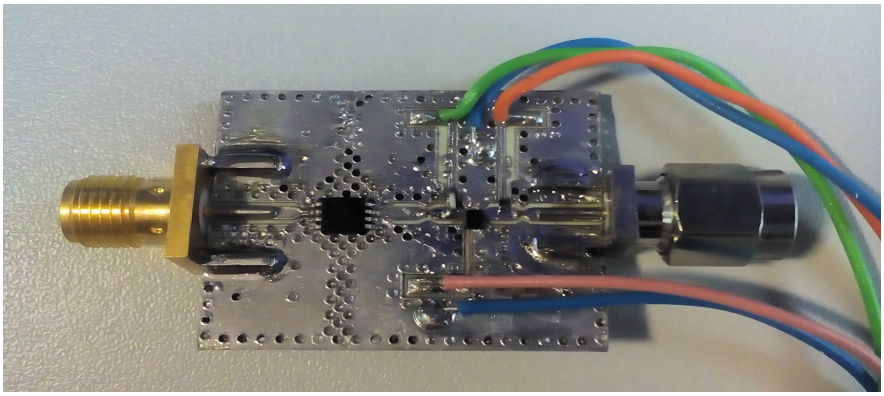


Figure 52 – Module B2 – 8 GHz to 16 GHz with output amplification.

4.6.3 – Module C – 16 GHz to 24 GHz active multiplier

For the last stage of multiplication the AMMP-6120 was included in the chain of module B1, for this module an adjustable brass support was constructed to hold the PCB and the 2,92 mm SMK connector. Figure 53 illustrates the Module C.

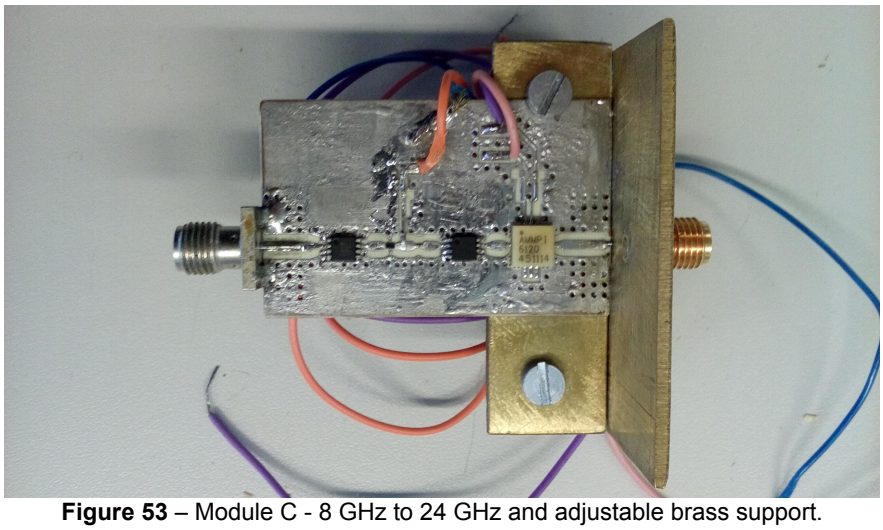


Figure 53 – Module C - 8 GHz to 24 GHz and adjustable brass support.

Unfortunately this module didn't work, and it is necessary to correct the problem.

4.6.4 – Frequency extension prototype modules summary and challenges

Table 11 summarizes the results of the output power of the frequency multipliers modules and the respective harmonic rejection,

Table 11 – Output power for modules A, B1 and B2 and respective harmonic rejection.

Module	**Output frequency** (GHz)	**Output power** (dBm)	**Harmonic rejection** (dBc)
A	4	11,336	16,794
	6	12,860	18,314
	8	10,441	17,658
B1	8	-3,247	8,208
	12	-2,225	16,026
	16	-8	5
B2	8	7,88	22,94
	12	6,91	27,42
	16	1,39	22,14

Although module B2 has a relative good performance for an unfiltered output, it depends on the module A and the results obtained for the frequency extension module B1 indicates that simply filtering won't work at this case, since the unwanted harmonic content is significantly high even without filtering. Filtering each section would require a significant number of high order filters in a multiplexing scheme (it is necessary to take into account that simple filtering may not be enough because of intermodulation problems). Creating a significant problem since passive diode balun mixers HMC189 and HMC204 conversion loss would rise on the desired bandwidth, because of the insertion losses of the filters. It would be necessary to find other VGAs capable to drive the passive doublers in order to solve the problem.

Even if the amplifiers were substituted, the design of distributed filters would require a significant area of the RF substrate and time for optimization. In order to get an idea figure 54 illustrates two cascaded 5th order Chebyshev low pass filters designed in the ADS software with a total length of 50 mm.

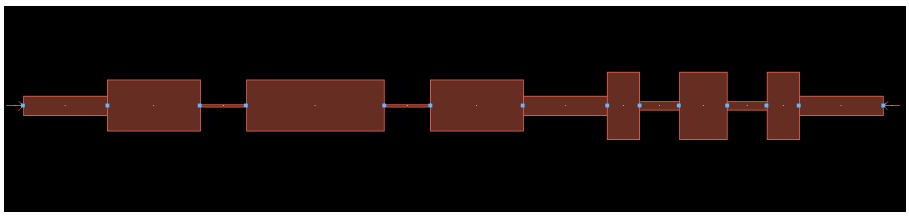


Figure 54 – Two cascaded Chebyschev low pass filters, designed in ADS 2011.

Each one of the filters were designed to have minimum insertion loss, the first one was designed to have a 0,5 dB pass band insertion loss with a cut off frequency at 5 GHz, and 30 dB insertion loss at 8 GHz. However when converting from lumped elements to microstrip lines its necessary to consider the manufacture restrictions, some can manufacture lines with a minimal width of 125 µm, the equivalent of a microstrip with a characteristic impedance of 124 Ω, for a 50 Ω system this would be the inductor element, and for a capacitance element a 7,6 mm width would result in a 12 Ω (such values were obtained using the line calculator of ADS 2011). In this case the higher impedance is still low for the first filter, instead of reaching a insertion loss of 30 dB at 8 GHz it only attenuates 20 dB, it would be necessary a different manufacture or a different substrate. The second filter was included to attenuate frequencies above 12 GHz, the two cascaded filters could be used at the input of the first frequency multiplier HMC189, it would allow to pass frequencies between 3 GHz and 4 GHz and attenuate the unwanted harmonics between 6 GHz to 16 GHz. The electromagnetic simulations for the two cascaded filters are illustrated in Figure 55.

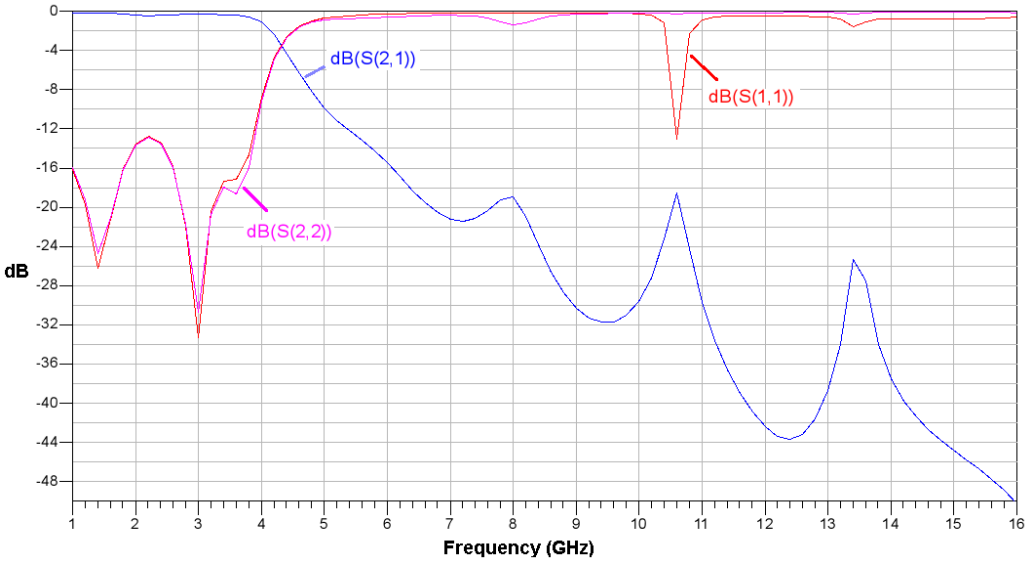


Figure 55 – Electromagnetic results for two cascaded filters.

To complement the input filtering section for the first multiplier a similar low pass filter could be used for the 2 GHz to 3 GHz input frequency, attenuating the unwanted harmonics between 4 GHz to 12 GHz, but this solution requires optimization and time. In order to solve the filtering problems a component search was realized. The manufacturer Mini-circuits has a family of high order filters that can cover frequencies from DC to 17 GHz, such filters can be used along with different VGAs and RF switches. Figure 56 illustrates one of the chains after the HMC189 doubler that was study in order to clear the unwanted harmonics for the HMC204 doubler.

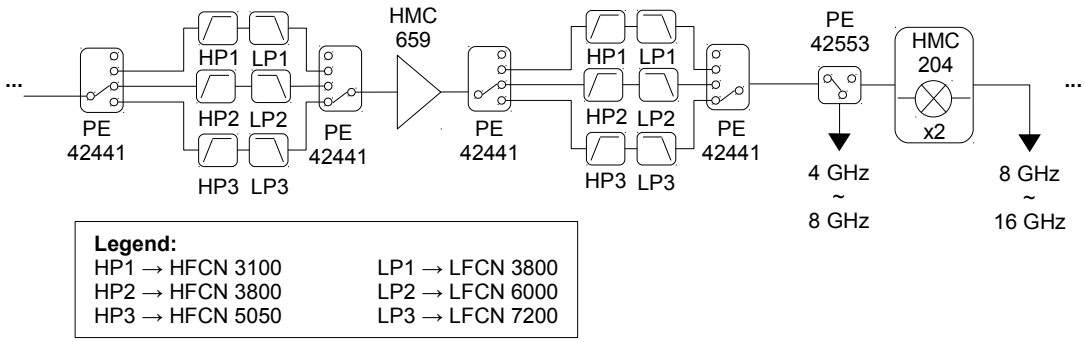


Figure 56 – Filtering section and amplification for the output band 4 GHz to 8 GHz.

However this solution doesn't ensures sufficient input power for the HMC204. Figure 57 shows the expected input power at the HMC204 doubler using CPWG lines with an electrical length of 180º and a 0,8 mm gap for 8 GHz.

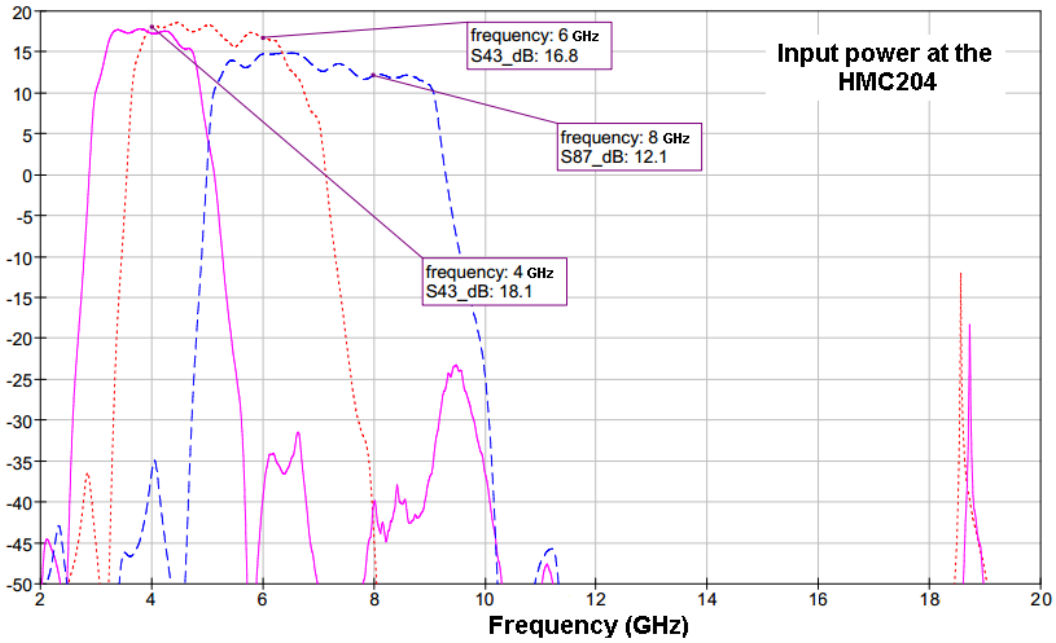


Figure 57 – Expected input power at the HMC204.

With the results obtained for the frequency extender study, it would be required to find other VGAs with a higher gain and implement a significant number of filters (for all bands). Because of that an alternative solution is presented in chapter 5 in order to reach the 24 GHz bandwidth, in order to minimize the complexity of the prototype.

Chapter 5 – Proposed architecture for future analysis

5.1 – Signal generator suggestion using the ADF5355

Instead of using the ADF435x IC family a similar IC can be used, the ADF5355 which is a signal source synthesizer with an internal doubler. The IC have 3 output ports, two of them covers the 54 MHz to 6,8 GHz band and the other the 6,8 GHz to 13,6 GHz. This minimizes the effort of the frequency extender circuit, with the possibility of achieving a 125 MHz of PFD (better phase noise performance). Figure 58 illustrates a block diagram that could be studied using the ADF5355.

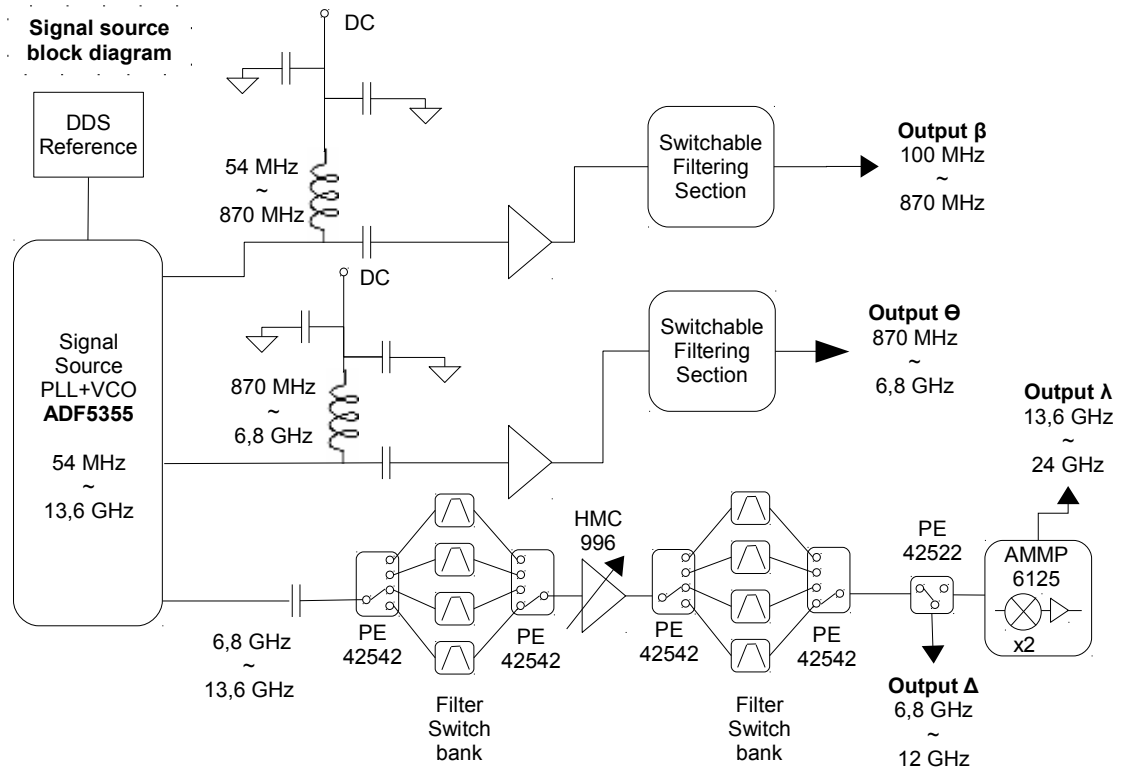


Figure 58 – Signal generator basic architecture using the ADF5355 IC.

In this architecture only one frequency doubler would be required to achieve the 24 GHz of bandwidth, the AMMP-6125, reducing the total number of ICs. Since the ADF5355 can achieve higher bandwidths, it is easier to filter the harmonics for the doubler AMMP-6125. The surface-mount filters from Mini-circuits and Marki Microwave would minimize the presence of the unwanted harmonics and clearing the thermal noise of the VGA HMC996 (5 GHz to 12 GHz bandwidth), which is responsible to guarantee the input power level to drive the doubler. Figure 59 shows the simulation results for the predicted input power at the active doubler, AMMP-6125, with CPWG lines, for an idealistic output power of 0 dBm of the ADF5355 (in reality the ADF5355 varies from 2 dBm to -6 dBm).

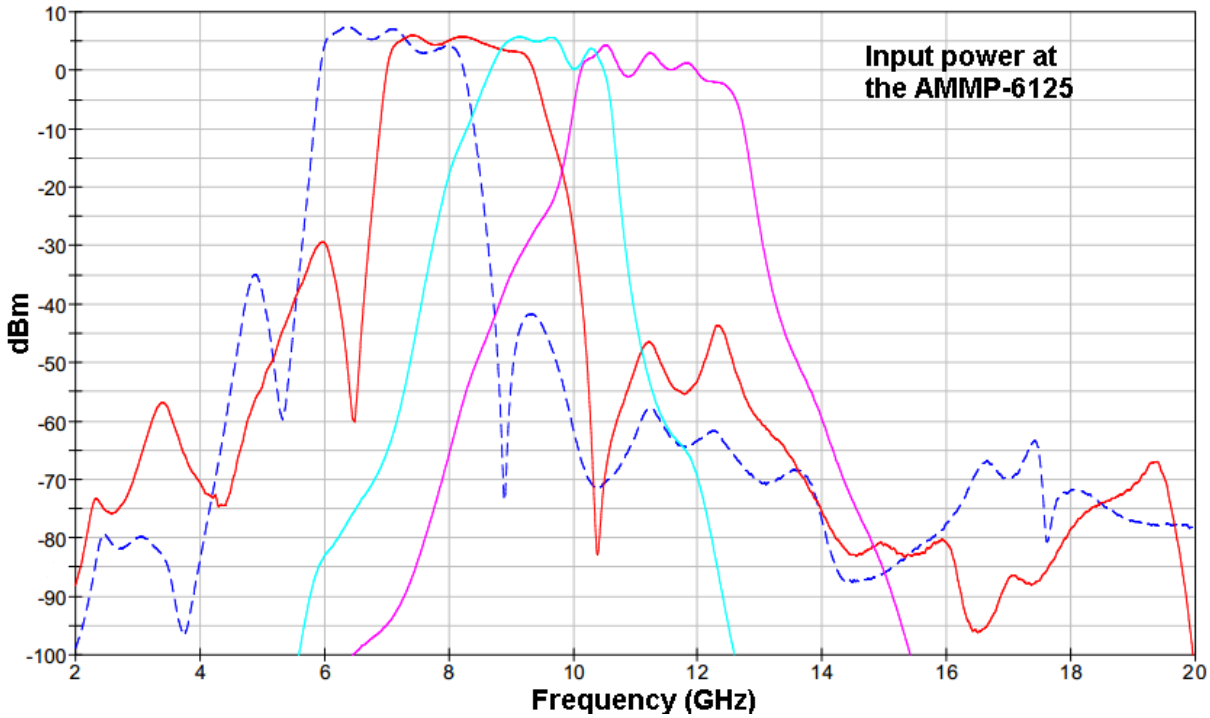


Figure 59 – Estimated input power at the doubler AMMP-6125.

The simulated results of Figure 59 indicates that there is sufficient power to drive the last active doubler. Compared to the active doubler AMMP-6120, the AMMP-6125 has a more stable output power along the bandwidth, even when the input power changes from -6 dBm to 4 dBm (ADF5355 output power varies along the bandwidth). Figure 60 illustrates the output power of the AMMP-6125.

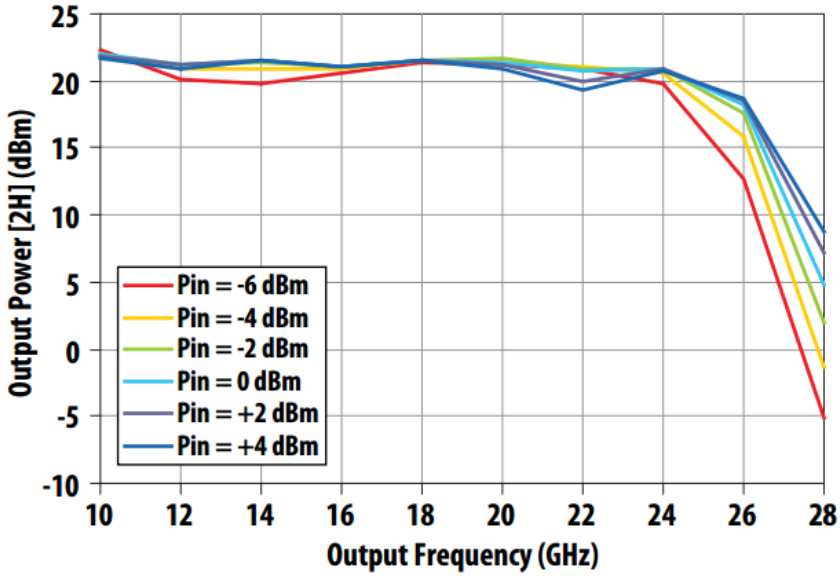


Figure 60 – Output Power of the doubler AMMP-6125, datasheet [18]

For the frequency band 54 MHz to 6,8 GHz, the filtering section could also be implemented with the RF switch HMC322ALP4E (SP8T version). And using the band pass filters from mini circuits. Tables 12 and 13 shows some pass band filters from mini circuits that may be relevant for attenuating the unwanted harmonics (bands 54 MHz to 870 MHz and 870 MHz to 6800).

Table 12 – Identified Mini-circuits pass band filters for cleaning the 54 MHz to 870 MHz band.

Filter model	BPF-C59+	RBP-98+	RBP-160+	RBP-253+	RBP-400+	BPF-C670+
Pass band Frequency (MHz)	54 to 88	88 to 131	131 to 210	210 to 340	340 to 490	490 to 870

Table 13 – Identified Mini-circuits pass band filters for cleaning the 870 MHz to 6,8 GHz band.

Filter model	BPF-A950+	BFCN-152W-75+	SYBP-2250+	BFCN-2975+	BFCN-3600+	BFCN-5100+
Pass band Frequency (MHz)	870 to 1200	1200 to 1970	1970 to 2620	2620 to 3440	3440 to 3900	3900 to 6800

Although this solution wasn't fully studied, compared to the first frequency extender architecture, it requires less effort to identify the various ICs to add output power for the frequency bands (54 MHz to 12 GHz). However it still requires caution, since temperature drifts could change the estimated input power at the AMMP-6125 doubler as well as mismatches between CPWG and ICs. If such happens it would be required to change the VGA HMC996, or add a second amplifier in the chain. Another aspect is the filters response at higher frequencies, although some manufactures provides the touchstone files the characterization doesn't always cover higher frequencies.

As seen in Figure 58 there’s a filter bank at the input of the VGA HMC996. That is necessary because of the poor harmonic rejection of the ADF5355 internal doubler (band 6,8 GHz to 13,6 GHz). Figure 61 illustrates the ADF5355 doubler output spectrum for 13,6 GHz.

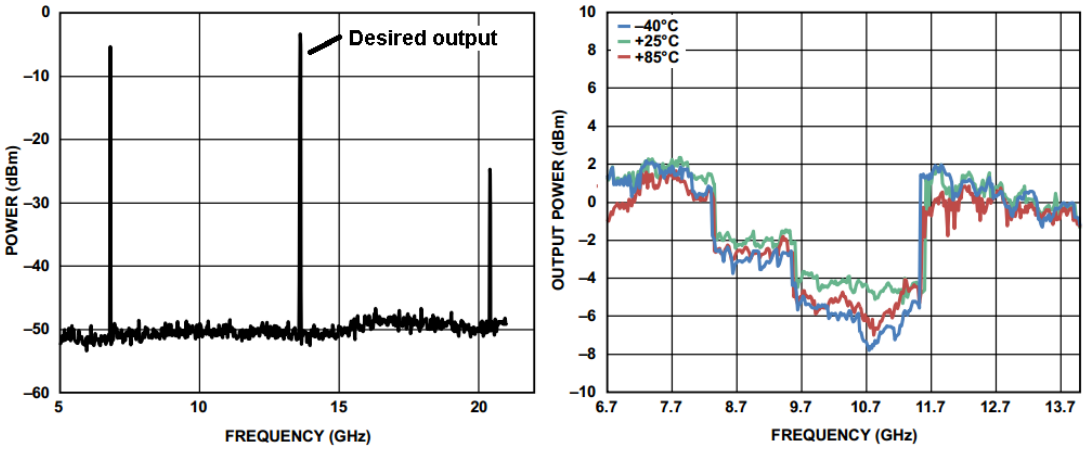


Figure 61 – ADF5355 doubler output power spectrum, adapted from [19]

But as seen in figure 59 the attenuation is significantly, for the unwanted harmonics relative to the passband 6,8 GHz to 12 GHz.

Another important aspect that also needs attention is the phase noise degradation. Amplifiers and multipliers can significantly degrade the phase noise. The phase noise that a multiplier introduces is given by

$$L(f_{out}) = L(f_{IN}) + 20Log_{10}N \quad (16)$$

(Note: N is the multiplication factor).

For amplifiers the phase noise degradation is strongly dependent on the bandwidth of the amplifiers, and in wideband amplifiers this can be a problem, if proper filtering isn't applied. The phase noise degradation of an amplifier is given by

$$L(f_{out}) = L(f_{IN}) + NF(dB) + kTB(dBm/Hz) - P_{IN}(dBm) \quad (17)$$

(Note: NF – Noise Figure; k – Boltzmann constant; T – temperature in Kelvin; B – bandwidth).

Although the architecture isn't complete, it was possible identify the ICs for driving the doubler AMMP-6125. The output power at the band 13,6 GHz to 24 GHz should round the 20 dBm, which is a considerable value since some Anritsu VNAs debit a -3 dBm output power at the ports (VNA MS46122A 1MHz to 43,5 GHz). It is necessary to take in account that there will be losses when the Test-and-Set for the DUT is implemented. As for the lower frequencies, below 12 GHz, it is necessary to find the amplifiers in order to have a similar output power. After that the 4 output ports could be orientated to a coaxial switch, such as the Keysight 87104D.

5.2 – Future implementations relative to the power leveling.

Once the signal source is capable to generate the output at all frequency bands it is necessary to adjust the output power, due to the necessity to calibrate the VNA. A suggestion for the power measuring is two use Shottky diodes. Figure 62 illustrates a power detection implementation using a “flat” detector with a matched pair of diodes [20].

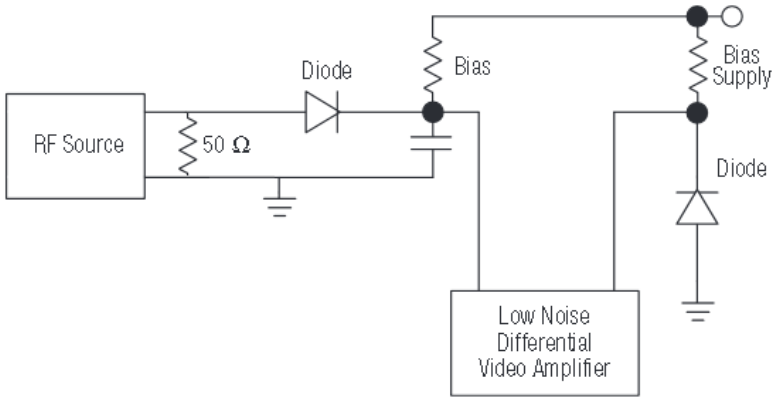


Figure 62 – Temperature compensated detector.

It wasn't possible to construct the power detector prototype, because of the mentioned problems at Section 3.2. However a brief explanation is presented for future development. As seen in Figure 62 there's a 50 Ω resistor to reduce the reflections between the detector and the RF source, this type of solution allows an extremely high bandwidth with low reflections (but with a degradation of the detector sensitivity) [20].

With the DC values from the video amplifier it would be possible to create a Look-Up-Table (LUT) in order to control a variable attenuator, per example AMMP-6650 (DC – 30 GHz), and with this the AGC module would be completed.

Chapter 6 – Conclusions

As seen in this work, VNAs are complex instruments that present significant challenges. Although was possible to prototype a signal generator, that covers a 35 MHz to 4,4 GHz of bandwidth with an output power that rounds the 5 dBm with the possibility to adjust the phase, which is an important feature for the homodyne sampler receiver.

A GUI was also developed to control the signal source, which aided the debugging process. As for the frequency extender prototypes it was only possible to reach up to 16 GHz. However the harmonic rejection of the frequency extender modules can be improved with proper filtering and layout techniques, but as mentioned in section 4.6.4 that would lead to a significant effort, since it would be necessary to reshape the architecture and find amplifiers with higher gain.

For that reason an alternative for signal generator prototype was suggested, using the IC ADF5355.

The following tasks summarizes the future work for the signal generator before considering the other circuitry for a VNA:

- Broadband matching between transmission lines and connectors, in order to minimize reflections between modules (DE-embedding the test fixtures);
- Explore the faster lock topology of the synthesizers ADF5355/ADF435x and the frequencies of comparison of the phase detector, considering the loop filter bandwidth, in order to minimize the phase noise (different step resolutions [5]);
- Implement a tunable reference signal, with a low phase noise DDS with a differential output (input reference of the ADF5355 is differential);
- Test if the mentioned filters of table 12 and 13 can be implemented, for the 54 MHz to 6,8 GHz band of the suggested signal source of section 5.1;
- Find amplifiers in order to obtain 20 dB of output power for the bands: 54 MHz to 870 MHz, 870 MHz to 6,8 GHz and 6,8 GHz to 12 GHz (section 5.1);
- Consider to implement a broadband prototype for the power detection, as suggested in section 5.2 (see reference [20]);

As for the other circuits that compose a VNA, the best solution is to separate them in frequency bands, since directional couplers have limited bandwidths.

For the down-conversion architecture a homodyne mixer-sampler is the easier solution. The mixer HMC773 (bandwidth 6 GHz to 26 GHz) can be used in the homodyne architecture.

The most difficult part may reside on the directional coupling devices, since this devices need rigorous manufacturing accuracy, however the alternative is to use a multi-section architecture (wider bandwidths) with a stripline implementation (requires a multilayer approach).

References

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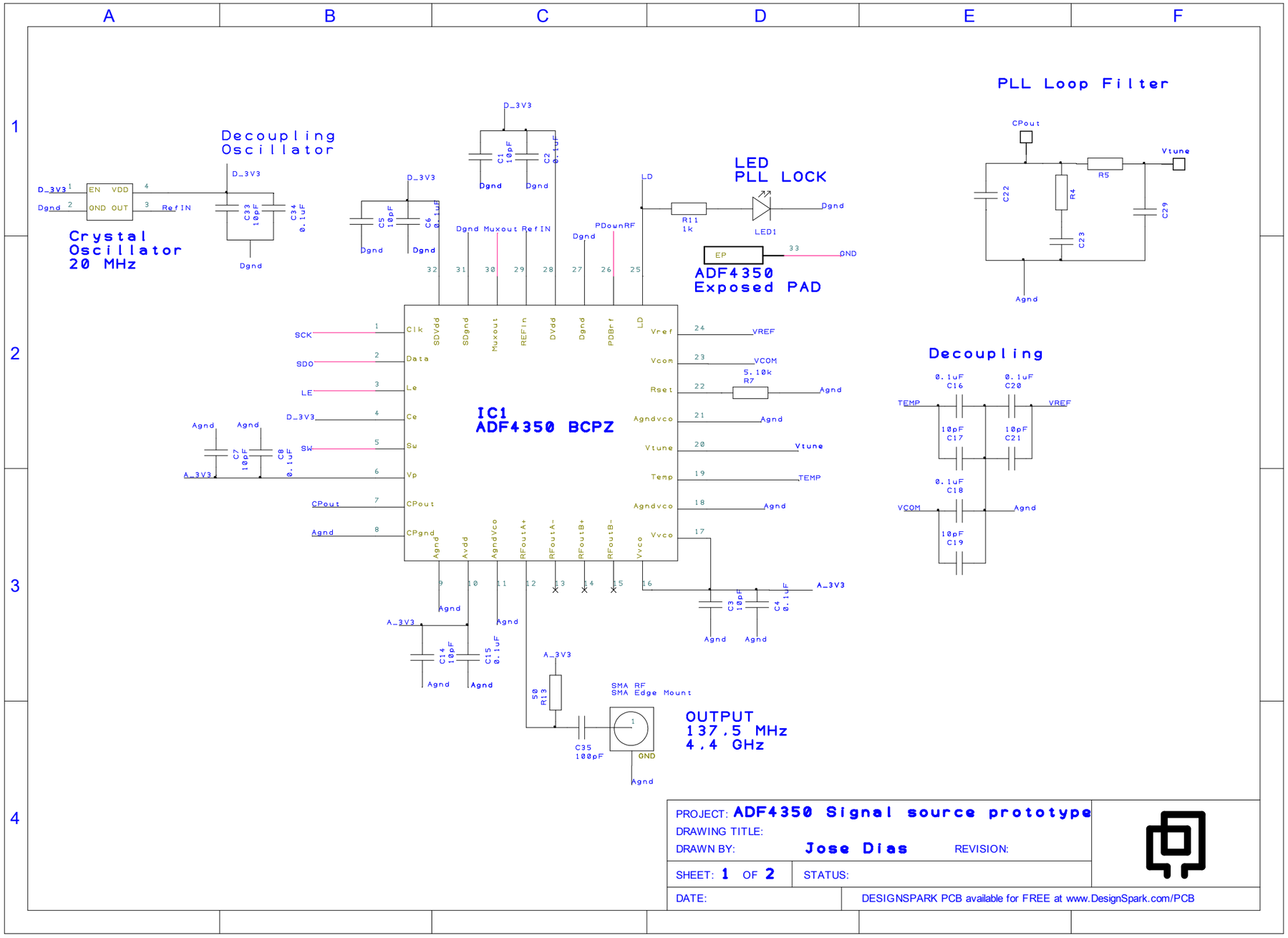
APPENDIX 1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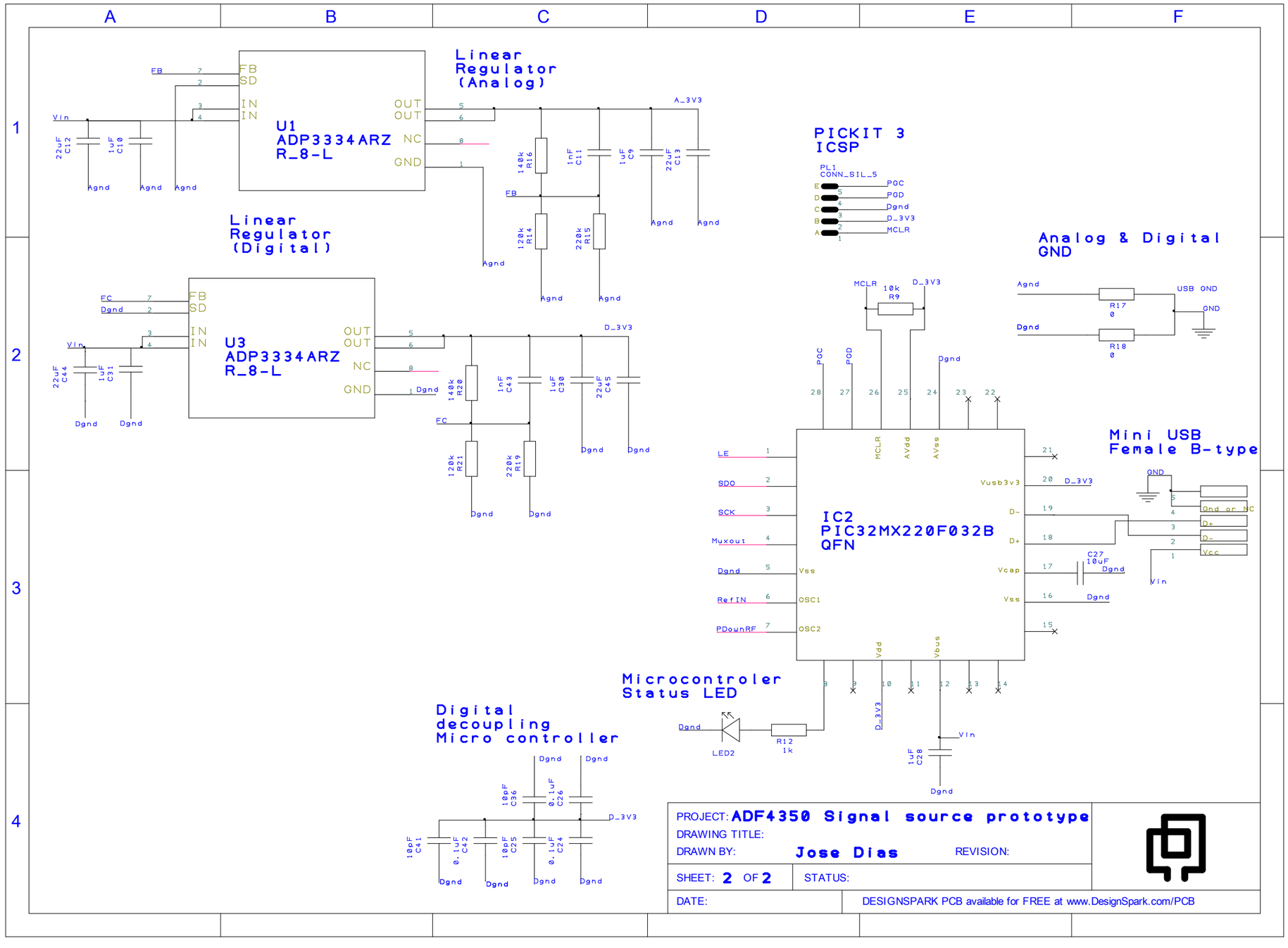
Crystal
Oscillator
20 MHz
LED
PLL LOCK
ADF4350
Exposed PAD
PLL Loop Filter
IC1
ADF4350 BCPZ
Decoupling
OUTPUT
137.5 MHz
4.4 GHz
SMA RF
SMA Edge Mount
PROJECT: ADF4350 Signal source prototype
DRAWING TITLE:
DRAWN BY: Jose Dias
REVISION:
SHEET: 1 OF 2
STATUS:
DATE:
DESIGNSPARK PCB available for FREE at www.DesignSpark.com/PCB

APPENDIX 2


Linear Regulator (Analog)
U1 ADP3334ARZ R_8-L
FB
SD
IN
IN
OUT
OUT
NC
GND
Vin
22uF C12
1uF C10
140k R16
1nF C11
1uF C9
22uF C13
A_3V3
120k R14
220k R15
Agnd
Linear Regulator (Digital)
U3 ADP3334ARZ R_8-L
FC
Dgnd
22uF C44
1uF C31
140k R20
1nF C43
1uF C30
22uF C45
D_3V3
120k R21
220k R19
PICKIT 3 ICSP
PL1 CONN_SIL_5
PGC
PGD
Dgnd
D_3V3
MCLR
Analog & Digital GND
USB GND
GND
R17 0
R18 0
10k R9
IC2 PIC32MX220F032B QFN
LE
SDO
SCK
Muxout
RefIN
PDownRF
Vss
OSC1
OSC2
MCLR
AVdd
AVss
Vusb3v3
D-
D+
Vcap
Vdd
Vbus
C27 10uF
C28 1uF
Mini USB Female B-type
Gnd or NC
Microcontroler Status LED
LED2
R12 1k
Digital decoupling Micro controller
10pF C36
0.1uF C26
10pF C41
0.1uF C42
10pF C25
0.1uF C24
PROJECT: ADF4350 Signal source prototype
DRAWING TITLE:
DRAWN BY: Jose Dias
REVISION:
SHEET: 2 OF 2
STATUS:
DATE:
DESIGNSPARK PCB available for FREE at www.DesignSpark.com/PCB