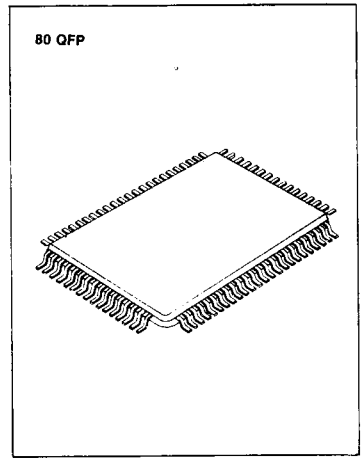
4-BIT MICROCONTROLLER

KS56C820 is an SMCS56, core-based 4-bit CMOS Microcomputer with LCD drivers, various peripherals that allows a high level of control of target products, and numerous I/O's. The flexible I/O control commands that can handle 1, 4, and 8 bit data manipulations will allow diverse applications control.

KS56C820 has enough LCD drivers, and many CPU clock modes that minimizes current that it is suitable for applications on portable products like CDPs, DATs, cameras and LCD remote controllers.



FEATURES

- Memory Mapped I/O
- ROM: 8064 x 8 bits
- RAM: 512 x 4 bits
- One 8-bit timer/counter input source: 2 external, and 4 internal inputs
- Watch timer
- One 8-bit SIO
  - — Can send either from LSB or MSB.
  - — Can choose either transmit and receive, or receive only modes
- Multiple vector interrupts
  - — Three external source interrupts: INT0, INT1, INT4
  - — Three internal source interrupts: Basic Timer, Timer/counter, SIO
  - — One external edge detectable quasi-interrupt: INT2
  - — One quasi-interrupt for clock: INTW
- 32 I/O bits (max 40 I/O bits)
  - — Inputs: 8 bits
  - — I/O: 16 bits: built-in LED driver.
  - — N-channel open drain I/O: 8 bitgs; can handle up to 10 volts.
  - — Output: Maximum 8 bits (including segment driver output)
- Max. 16 digits of LCD driver
  - — Static, 1/2, 1/3, 1/4 duty selectable.
  - — 24, 28, 32 segment output selectable.
- 2KHz output for buzzer
- 16-bit Bit Sequential Carrier useful for remote controller.
- Two types of power-down modes
  - — Idle: Only the CPU clock stops.
  - — Stop: All internal clocks stop.
- Can choose from various instruction cycle times for power saving.
  - — Using Main-system clock: 1, 2, 16μS/4MHz
  - — Using Sub-system clock: 122μS/32.768KHz
- Built-in crystal/ceramic oscillator circuits for clock.
  - — Crystal/ceramic oscillator circuit for main-system clock.
  - — Crystal oscillator circuit for sub-system clock.
- 3/5V single power supply
- 80 Plastic Quad Flat Package

PIN CONFIGURATION

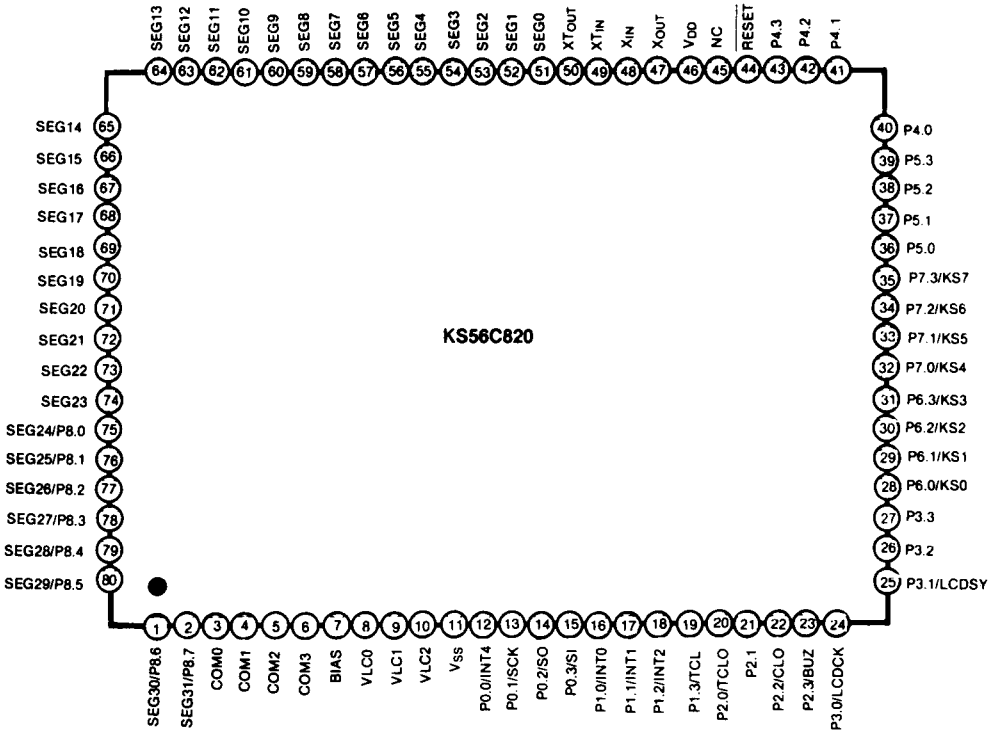


Fig. 1

PIN DESCRIPTION

Symbol	Description	
P1.0-P1.3	4-bit Input	Internal pull-up resistor can be specified in 4-bit unit by software
P2, P7	4-bit Input/Output	
P3, P6	I/O mode selectable in 1-bit unit by software	
P4, P5	4-bit input/output, N-ch open drain	
P8.0-P8.7	Outputs in 1-bit unit (shared with segment outputs)	
SEG0-SEG23	Segment output for LCD display	
SEG24-SEG31	Segment output for LCD display (shared with Port 8)	
COM0-COM3	Common signal output for LCD display	
VLC0-VLC2	LCD power supply pin	
BIAS	LCD power supply control pin for 3/5V operating	
LCDCK	LCD clock output for display expansion	
LCDSY	LCD sync. clock output for display expansion	
TCL	Timer/Counter external clock input	
TCLO	Timer/Counter clock output	
INT0, 1, 2, 4	External interrupt input	
CLO	Clock output	
BUZ	2KHz clock output for buzzer	
KS0-KS7	Semi-interrupt input detecting external falling edge	
SCK, SI, SO	SCK: serial clock, SI: serial input, SO: serial output	
X_{IN}, X_{OUT}	Crystal/Ceramic or RC clock I/O for Main-system clock	
XT_{IN}, XT_{OUT}	Crystal clock I/O for sub-system clock	

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Test Conditions		Value	Unit
Supply Voltage	V_{DD}			−0.3 ~ +7.0	V
Input Voltage	V_I			−0.3 ~ V_{DD} + 0.3	V
Output Voltage	V_O			−0.3 ~ V_{DD} + 0.3	V
High Output Current	I_{OH}	1 Port		−15	mA
		All Ports		−30	mA
Low Output Current	I_{OL}	1 Port	MAX.	30	mA
			TYP.	15	mA
		Port 2, Port 3	MAX.	100	mA
			TYP.	60	mA
		Port 6	MAX.	100	mA
			TYP.	60	mA
Operating Temperature	T_{OPR}			−20 ~ +75	°C
Storage Temperature	T_{STG}			−55 ~ +125	°C

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Ta = −40 ~ +85°C, V_{DD} = 4.0 ~ 6.0V)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
High Input Voltage	V_{IH1}	Port 2, 3		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Port 1, 6, RESET		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Port 4, 5	built in pull up re-	0.7 V_{DD}		V_{DD}	V
			-sistor open drain	0.7 V_{DD}		10 V_{DD}	V
	V_{IH4}	X_{IN}, X_{OUT}, XT_{IN}		V_{DD} − 0.5		V_{DD}V	
Low Input Voltage	V_{IL1}	Port 2, 3		0		0.3 V_{DD}	V
	V_{IL2}	Port 1, 6, RESET		0		0.2 V_{DD}	V
	V_{IL3}	X_{IN}, X_{OUT}, XT_{IN}		0		0.4	V
High Output Voltage	V_{OH1}	Port 2, 3, 6, BIAS	I_{OH} = −1mA	V_{DD} − 1.0			V
			I_{OH} = −100μA	V_{DD} − 0.5			V
	V_{OH2}	P8.0-7	I_{OH} = −100μA	V_{DD} − 2.0			V
			I_{OH} = −30μA	V_{DD} − 1.0			V
Low Output Voltage	V_{OL1}	Port 2, 3, 6, BIAS	I_{OL} = 15mA		0.4	2.0	V
			I_{OL} = 1.6mA			0.4	V
			I_{OL} = 400μA			0.5	V
	V_{OL2}	P8.0-7	I_{OL} = 100μA			1.0	V
			I_{OL} = 50μA			1.0	V
Supply Current	I_{DD1}	4.19MHz	V_{DD} = 5V + 10%		2.5	8	mA
			V_{DD} = 3V + 10%		0.35	1.2	mA
	I_{DD2}		IDLE V_{DD} = 5V		500	1500	μA
			IDLE V_{DD} = 3V		150	450	μA
	I_{DD3}	32.768 KHz	V_{DD} = 3V + 10%		30	90	μA
	I_{DD4}		IDLE V_{DD} = 3V		5	15	μA

AC CHARACTERISTICS (Ta = −40 ~ +85°C, V_{DD} = 4.0 ~ 6.0V)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Cycle Time	t_{CY}	Main-system Clock	0.95		64	μS
		Sub-system Clock	114	122	125	μS
TCL Input Frequency	$f_{I(TCL)}$	V_{DD} = 4.5 ~ 6.0V	0		1	MHz
			0		275	KHz
TCL Input High & Low Level Width	$t_{WIH}/t_{WIL\ 1}$	V_{DD} = 4.5 ~ 6.0V	0.48			μS
			1.8			μS
Ext. Interrupt High & Low Level Width	$t_{WIH}/t_{WIL\ 2}$					μS
		INT1, INT2	10			μS
		KS0 − KS3	10			μS
RESET Low Level Width	$t_{WL(RST)}$		10			μS