SECTION 3
TESTING DIODES

3.1 THE SEMICONDUCTOR DIODE AND ITS CHARACTERISTICS

3.1.1 Diode Symbol and Definition

A semiconductor diode is formed by the creation of a junction between P-material and N-material within a crystal during the manufacturing process. The standard semiconductor diode has in its symbol, an arrow to indicate the direction of forward current flow, as shown in Figure 3-1. With positive voltage applied to the P-material and negative voltage applied to the N-material, the diode is said to be forward biased, as shown in Figure 3-2. The current (I_f) increases rapidly with small increases in applied voltage (V).

When the applied voltage is reversed, the P-material is negative with respect to the N-material, and very small levels of current flow through the diode. The small current (I_o) is the diode "reverse saturation current," and its magnitude increases with temperature. In practice, I_o can be ignored.

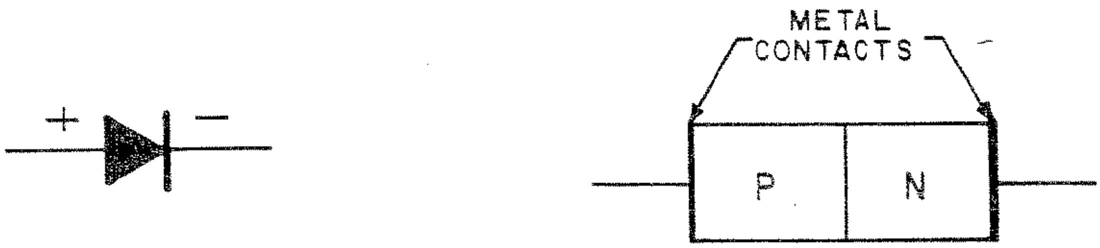


Figure 3-1. Diode Symbol

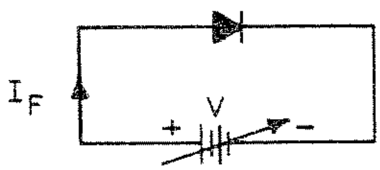


Figure 3-2. P-N Junction
Biased in the Forward Direction

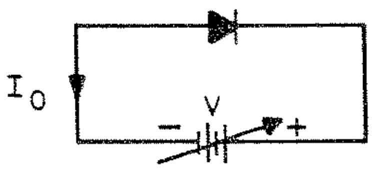


Figure 3-3. P-N Junction
Biased in the Reverse Direction

3.1.2 The Volt-Ampere Characteristic

For a P-N junction, the current (I) is related to the voltage (V) by the following equation:

$$I = I_o (\exp kV\text{-}1)$$

Where k is a constant depending on the temperature and material. The volt-ampere characteristic described by the equation above is shown in Figure 3-4. For the sake of clarity, the current (I_o) has been greatly exaggerated in magnitude. The dashed portion of the curve in Figure 3-4 indicates that, at a certain reverse voltage (V_{br}), the diode characteristic exhibits an abrubt and marked departure from the equation above. At this critical voltage, a large reverse current flows and the diode is said to be in the "breakdown region."

3.2 SILICON RECTIFIER DIODES

3.2.1 Signatures of a Good Diode

A good diode has very large reverse biased resistance and small forward biased resistance. The forward junction voltage drop (V_f) is between 0.5 Volts and 2.8 Volts depending on the semiconductor material. For example, V_f is 0.6 Volts for a silicon diode, and V_f is 1.5 Volts for a typical light-emitting diode. The Tracker 2000 can visually display all these parameters.

Figure 3-5 shows the Tracker 2000 connections for diode testing. Figure 3-6 shows typical signatures (low, medium 1, medium 2, and high range) and waveforms, plus the circuit equivalent for a good silicon diode. The forward junction voltage drop of a diode can be determined (approximately) from the low range signature.

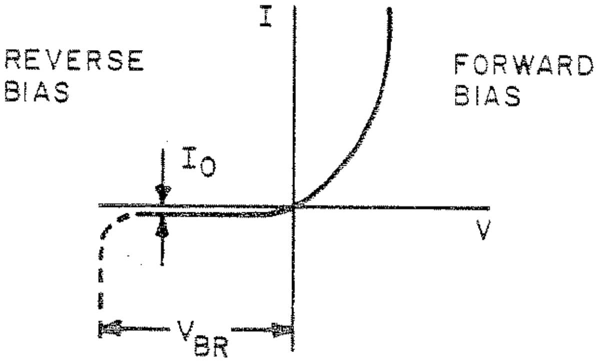


Figure 3-4. The Volt-Ampere Characteristic of a Semiconductor

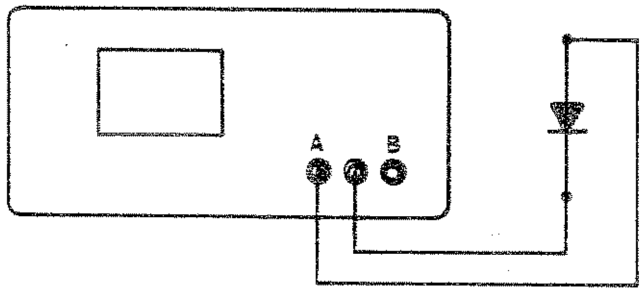


Figure 3-5. Tracker Test Circuit

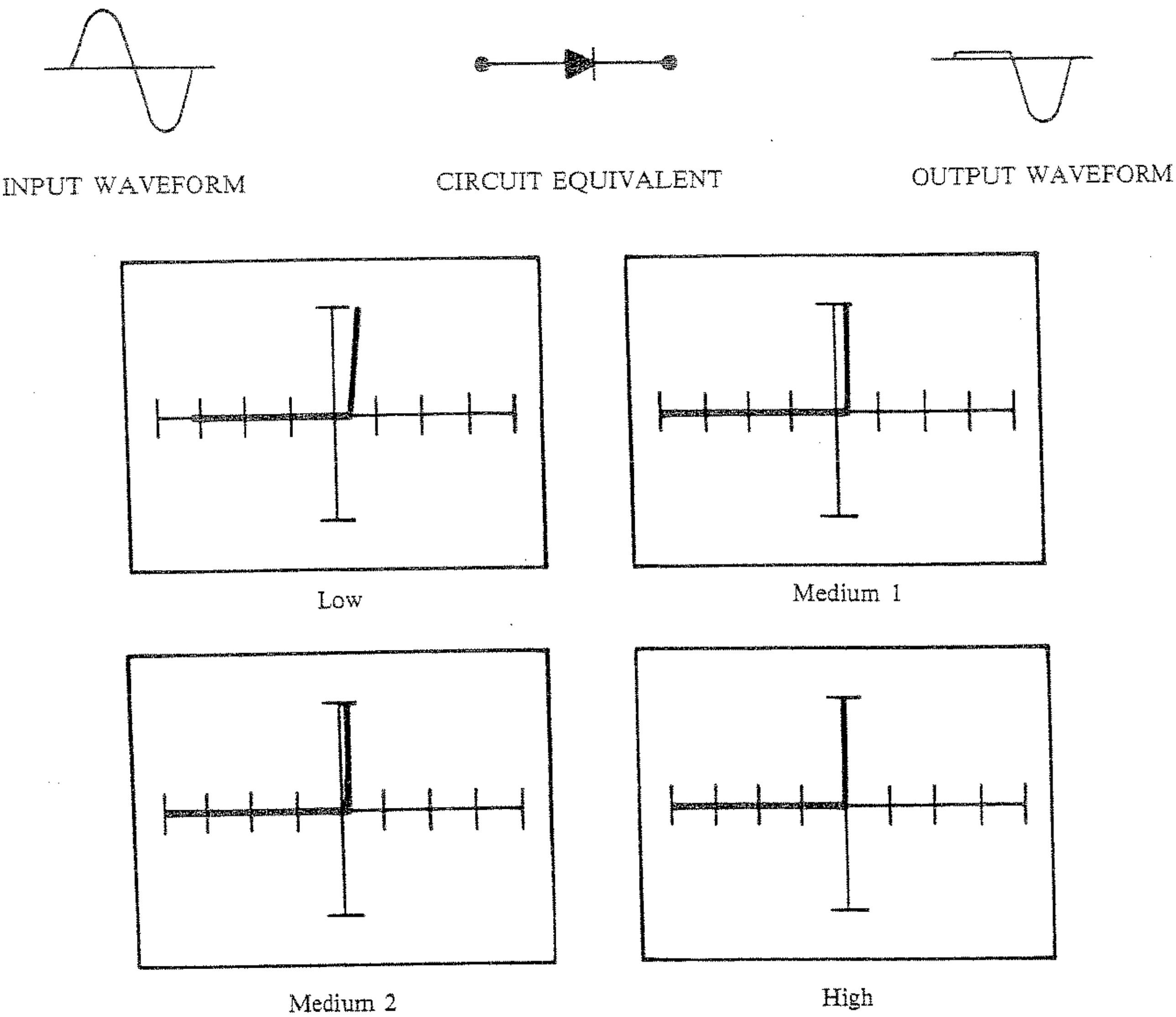


Figure 3-6. Signatures of a Silicon Diode at 60Hz

3.2.2 Signatures of Defective Diodes

A rectifier diode is defective if it is open, is shorted (low impedance), contains high internal impedance, or contains leakage. Figure 3-7 shows the patterns of an "open" diode in all ranges.

The Tracker 2000 is capable, in the low range, of detecting resistance higher than one ohm, and this resistance causes the vertical trace to rotate in a clockwise direction. The angle of rotation is a function of the resistance. Figure 3-8 shows the effect of circuit resistances on the trace rotation while in the low range. This small short circuit resistance does not cause rotation in the medium 1, medium 2 and high ranges of the Tracker 2000.

Figure 3-9 shows the waveforms, circuit equivalent and signatures of a diode that exhibits a nonlinear resistance in series with the diode junction. This resistance effects the ability of the diode to turn on at the proper voltage, and causes excessive heat dissipation.

In low range, the Tracker 2000 is capable of detecting series resistance as low as 1 ohm. However, Medium 1 range is only capable of detecting such resistance higher than 50 ohms.

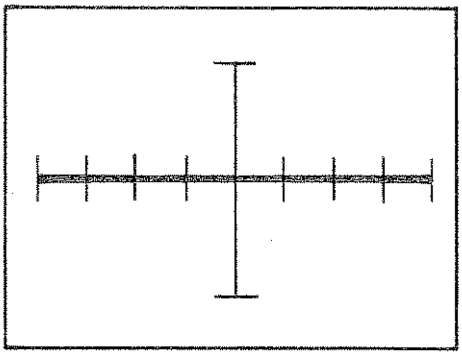


Figure 3-7. Signature of an Open Diode

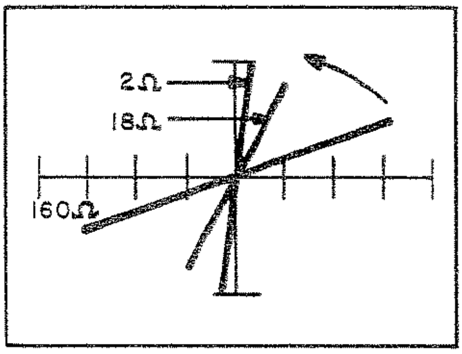
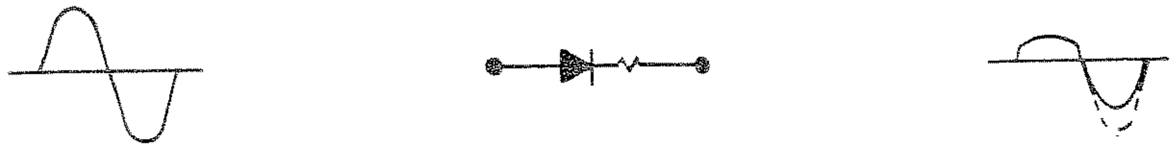
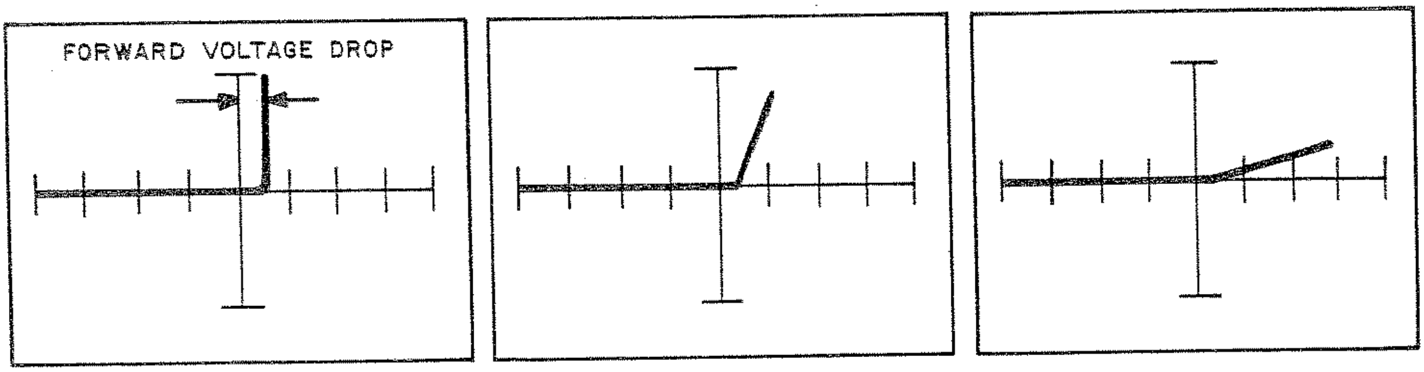


Figure 3-8. Effect of Resistance on the Tracker 2000 Signature in Low Range at 60Hz



INPUT WAVEFORM | CIRCUIT EQUIVALENT | OUTPUT WAVEFORM

R = 0 ohm | R = 10 ohm | R = 100 ohm



Good 1N4001 Diode | 1N4001 with 10 ohm series resistance | 1N4001 with 100 ohm series resistance

Figure 3-9a. Signature Deviation from a Good Diode in Low Range at 60Hz

R = 0 ohm | R = 10 ohm | R = 100 ohm

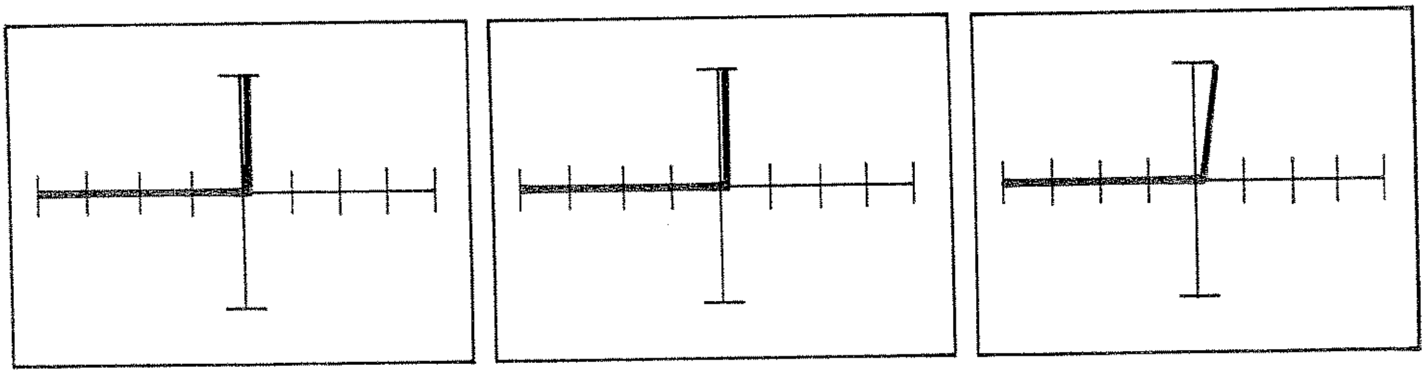
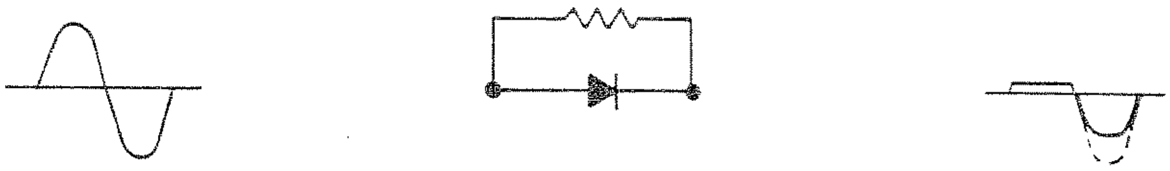


Figure 3-9b. Signature Deviation from a Good Diode in the Medium 1 Range at 60Hz

Figure 3-10 shows the waveforms, circuit equivalent and signatures of a diode that exhibits a nonlinear resistance in parallel with the diode junction (leaky) when reverse biased. This resistance effects the ability of the diode to provide maximum output for a given input.



INPUT WAVEFORM | CIRCUIT EQUIVALENT | OUTPUT WAVEFORM

Figure 3-10a. Model of Diode with Leakage Resistance of R

No Leakage | R = 100 ohm | R = 1K

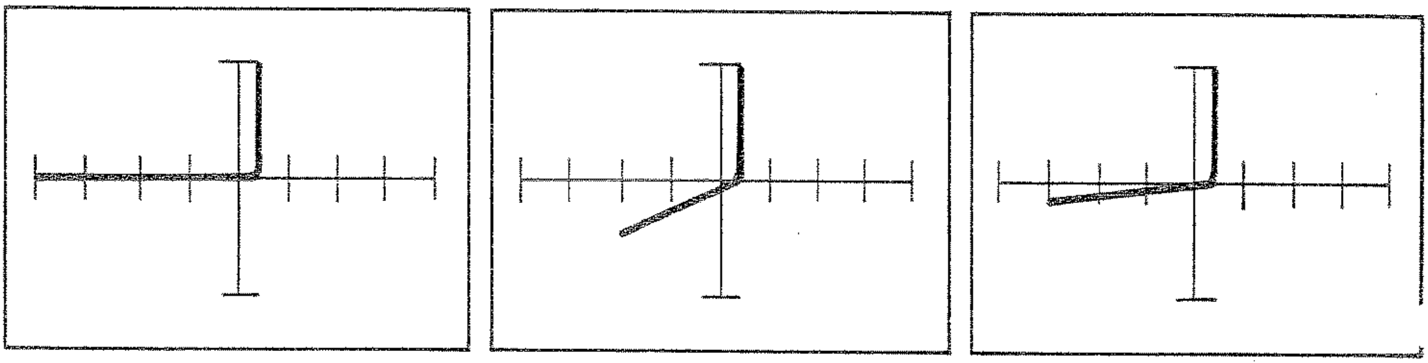


Figure 3-10b. Influence of Leakage Resistance in Low Range at 60Hz.

No Leakage | R = 1K | R = 10K

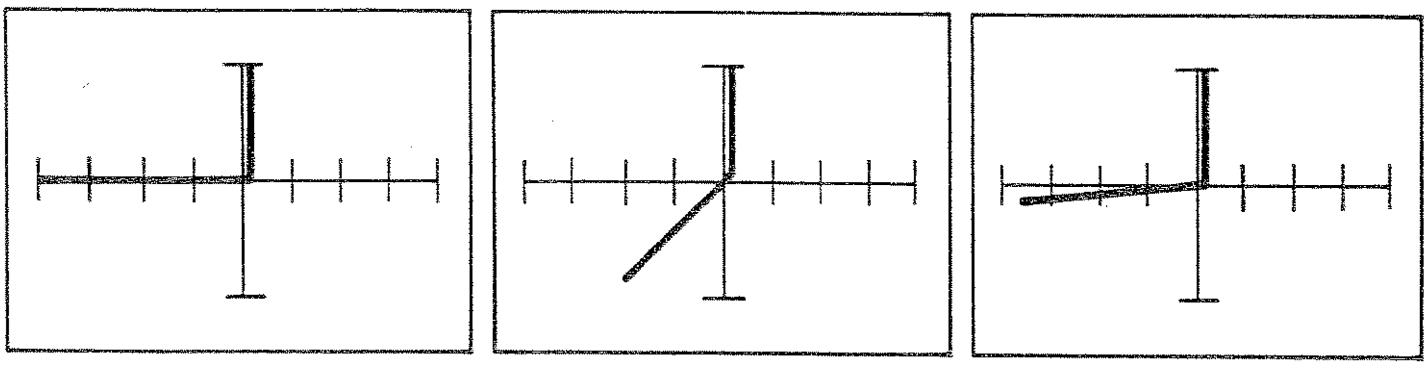


Figure 3-10c. Influence of Leakage Resistance in Medium 1 Range at 60Hz.

No Leakage R = 10K R = 100K

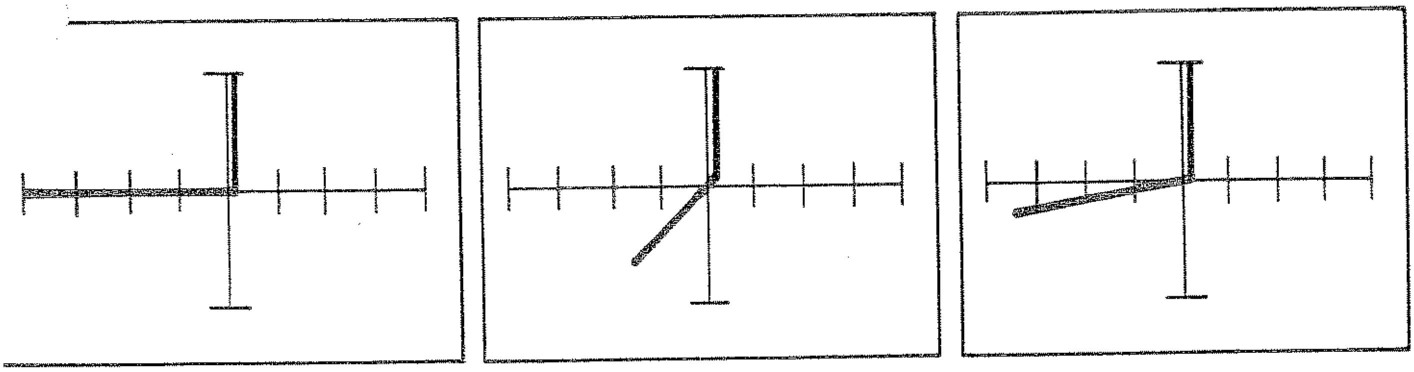


Figure 3-10d. Influence of Leakage Resistance in Medium 2 Range at 60Hz.

No Leakage R = 100K R = 1 Meg

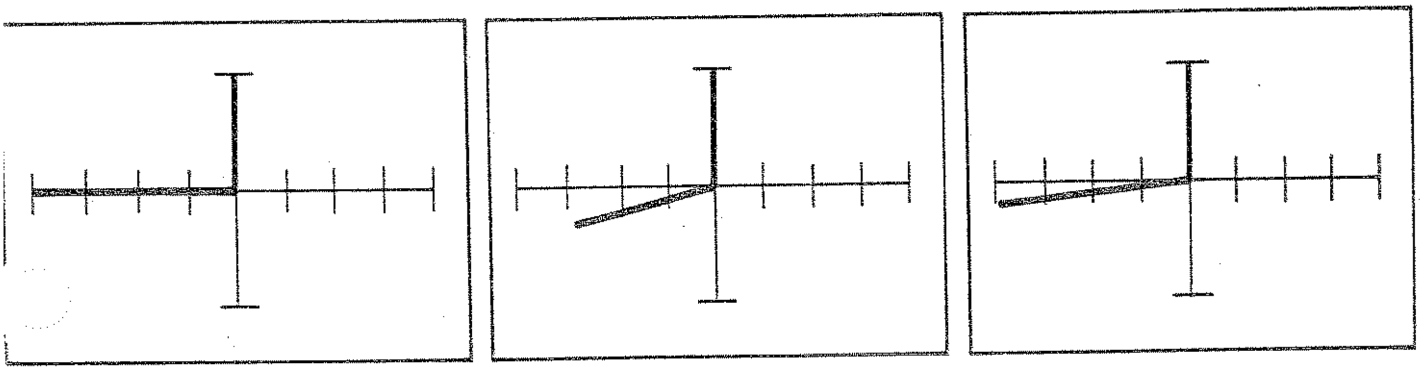
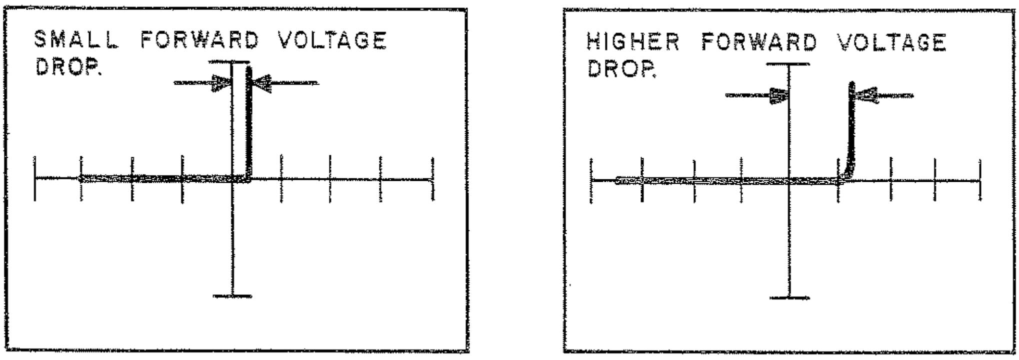


Figure 3-10e. Influence of Leakage Resistance in High Range at 60Hz

The Tracker 2000 is capable of detecting leakage resistance with values between 1 ohm to 2 Megohms.

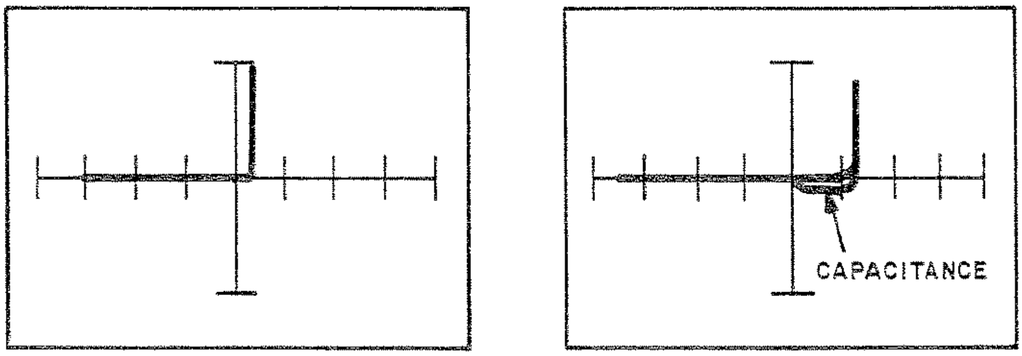
3.3 HIGH VOLTAGE SILICON DIODES

High voltage diodes are tested in the same manner as that described for rectifier diodes in section 3.2. High voltage diodes, such as the HV15F, display higher forward voltage drop (V_f) than low voltage diodes because the doping is different and the diode junction is required to withstand the rated high voltage. High voltage diodes also exhibit higher junction capacitance. This capacitance is most easily viewed when using the 2KHz test frequency. Figures 3-11 a and b show the signatures of a 1N4001 and a high voltage diode HV30 (3KV breakdown) when they are tested at 60Hz and 2KHz respectively.



IN4001 HV30

Figure 3-11a. Signatures of a 1N4001 and an HV30 in Low Range at 60Hz



1N4001 HV30

Figure 3-11b. Signatures of a 1N4001 and an HV30 in Low Range at 2KHz

3.4 RECTIFIER BRIDGES

A rectifier bridge assembly is made up of four diodes configured as shown in Figure 3-12. Points A and B are the AC power input terminals, and points C and D are the positive and negative output terminals, respectively. To test the bridge, the Tracker 2000 is connected to terminals A and B as shown in Figure 3-12.

A good bridge appears as an open circuit to the Tracker 2000 because the diodes are reverse biased. Figure 3-13 shows the signatures produced by a good bridge with the Tracker 2000 connected across points A and B. Figure 3-14 shows the signatures produced by a bridge with either diode D2 or D4 shorted, while Figure 3-15 shows the signatures produced with either diode D1 or D3 shorted.

Figure 3-16 shows the test connections of the Tracker 2000 to the positive and negative terminals of the rectifier bridge. Channel A is connected to the positive terminal, and common is connected to the negative terminal. Figure 3-17 shows the signatures of a good bridge when connected as shown in Figure 3-16.

Figure 3-18 shows a reversal of the test connections shown in Figure 3-16. Figure 3-19 shows the signatures resulting from the reversal of the test connections to the bridge.

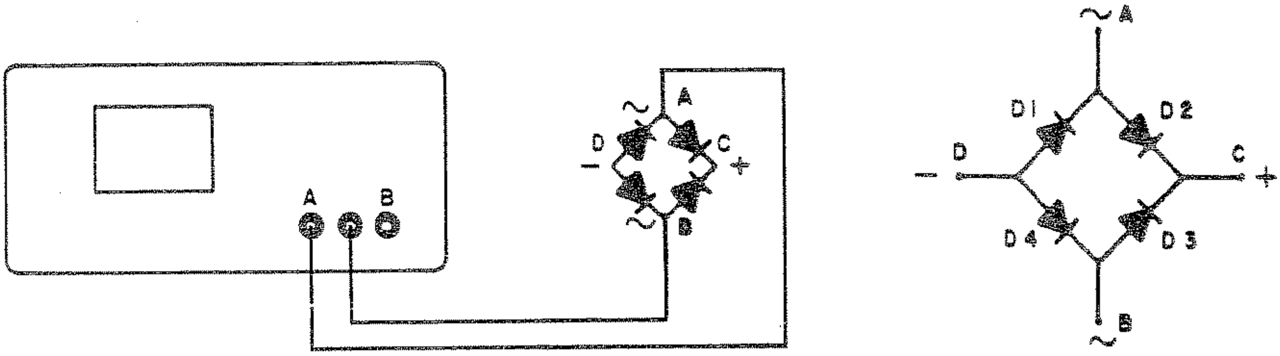


Figure 3-12. Rectifier Bridge Test Connections — AC Input

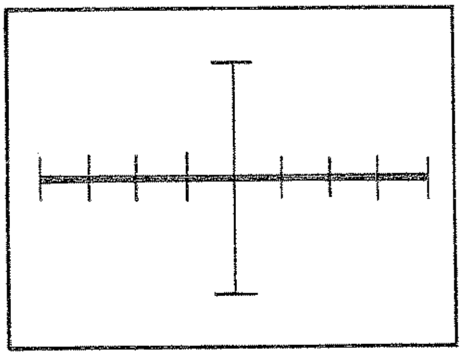


Figure 3-13. Patterns of a Good Rectifier Bridge

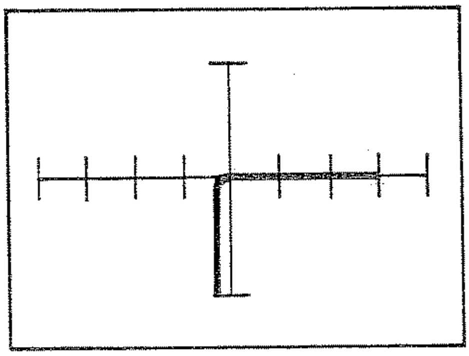


Figure 3-14. Signature with D2 or D4 Shorted in Low Range at 60Hz

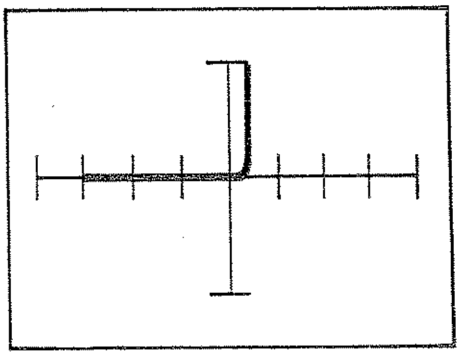


Figure 3-15. Signature with D1 or D3 Shorted in Low Range at 60Hz

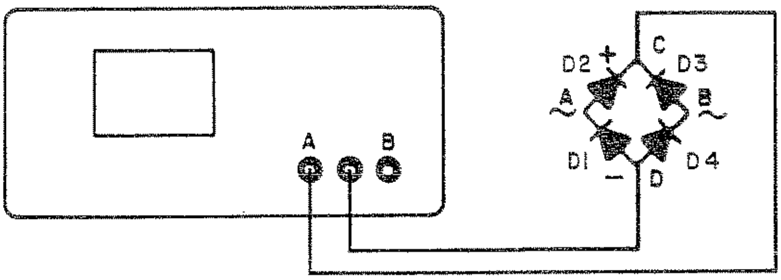


Figure 3-16. Rectifier Bridge Connections — DC Output

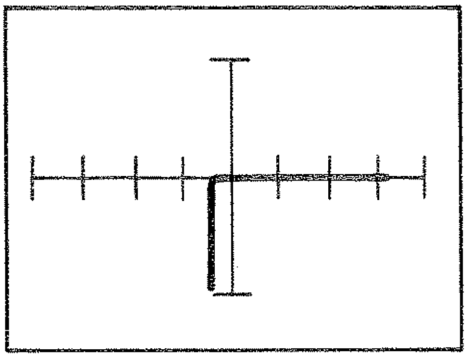


Figure 3-17. Signature of the DC Output in Low Range at 60Hz

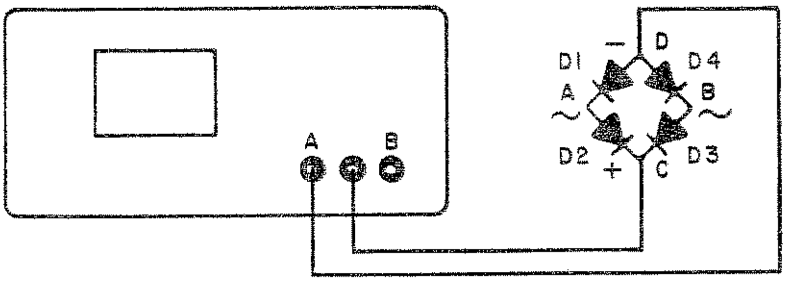


Figure 3-18. Rectifier Bridge, Reversed Test Connections

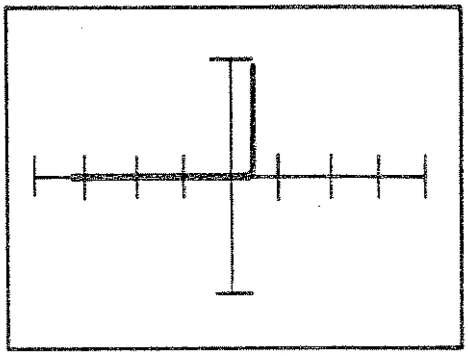
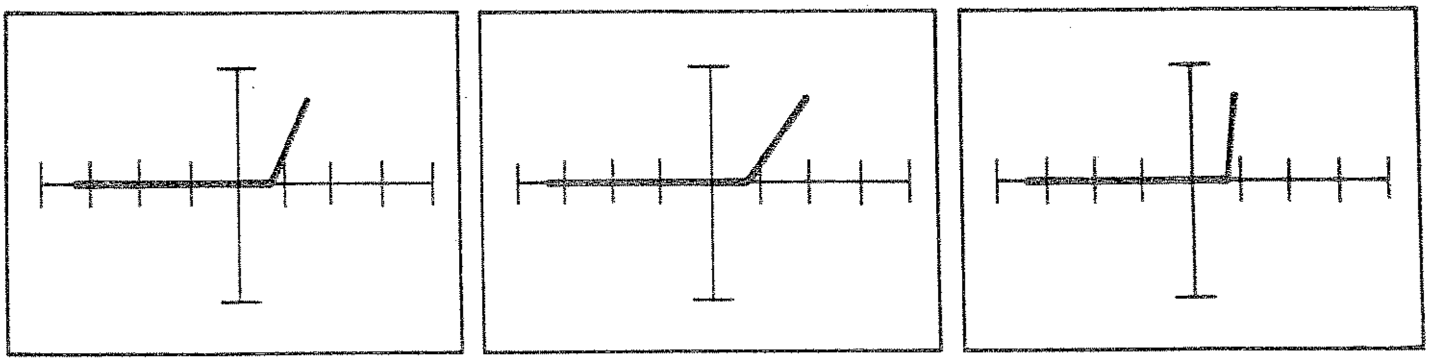


Figure 3-19. Signature with the DC Output Reversed in Low Range at 60Hz

3.5 LIGHT-EMITTING DIODES

Light-emitting diodes (LEDs) may be tested with the Tracker 2000 by using the low range and connecting the probes across the LED. A good LED provides an adequate amount of light as a result of the Tracker 2000 connections. Figure 3-20 shows the signatures for different colored LEDs, each of which exhibit different forward voltages (V_f).



COLOR: RED
RANGE: LOW

COLOR: AMBER
RANGE: LOW

COLOR: GREEN
RANGE: LOW

Figure 3-20. LED Signatures

3.6 ZENER DIODES

The zener diode is unique among the semiconductor family of devices in that its electrical properties are derived from a rectifying junction which operates in the reverse breakdown region. Figure 3-21 shows the volt-ampere characteristics of a typical 30 Volt zener diode.

Figure 3-21 shows that the zener diode conducts current in both directions, with the forward current being a function of the forward voltage. Note that the forward current is small until the forward voltage is approximately 0.65V, then the forward current increases rapidly. When the forward voltage is greater than 0.65V, the forward current is limited primarily by the circuit resistance external to the diode.

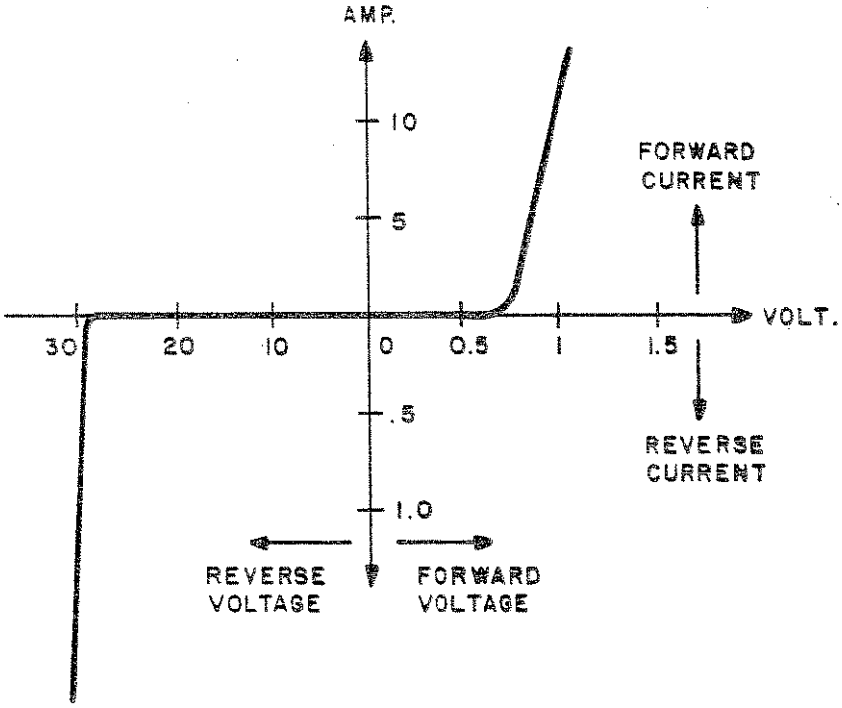


Figure 3-21. Characteristics of a Typical 30V Zener Diode

The reverse current is a function of the reverse voltage and, for most practical purposes, is zero until such time as the reverse voltage equals the P-N junction breakdown voltage. At this point the reverse current increases rapidly. The P-N junction breakdown voltage (V_Z) is usually called the zener voltage. Commercial zener diodes are available with zener voltages from about 2.4V to 200V. The Tracker 2000 displays the zener diode breakdown voltage (V_Z) on the display.

Figure 3-22 shows the Tracker 2000 connections to a 1N5242 zener diode, a 12 Volt device. Figure 3-23 shows the signatures produced by the zener diode.

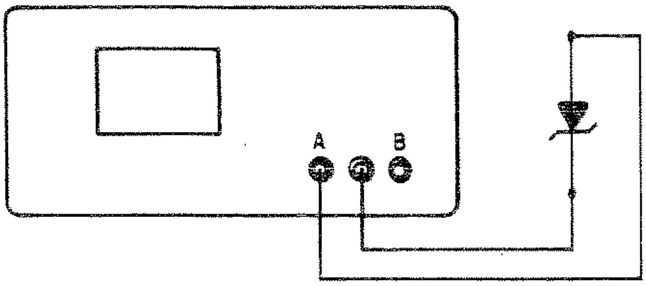
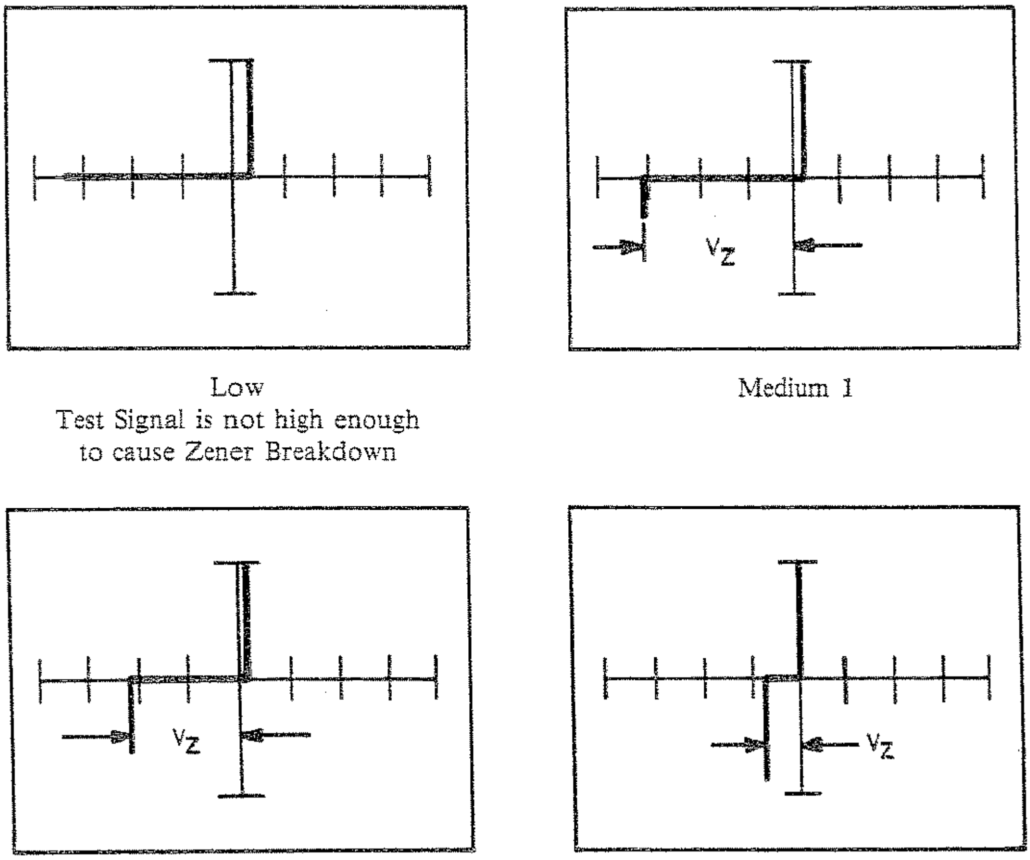


Figure 3-22. Zener Diode Test Connections



Low
Test Signal is not high enough
to cause Zener Breakdown

Medium 1

Medium 2

High

Figure 3-23. Signatures of a 1N5242 Zener Diode at 60Hz

In the low range, the Tracker 2000 test signal at the probes is 20 Volts peak to peak, and is insufficient to cause zener breakdown for the 1N5242. As a result, the signature looks identical to that of a general purpose diode such as a 1N4001. However, in the medium 1 range, the Tracker 2000 test signal is 30 Volts peak to peak and the zener voltage (V_Z) can be seen.

A good zener diode gives a sharp, well-defined signature of zener breakdown voltage, while an inferior zener device gives a signature with a rounded corner. (Refer to Figures 3-24 and 3-25).

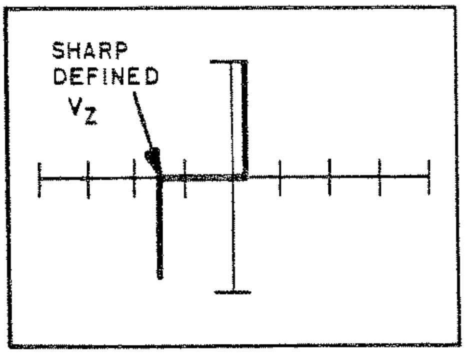


Figure 3-24. Signature of a Good Zener Diode in the Medium 1 Range at 60Hz

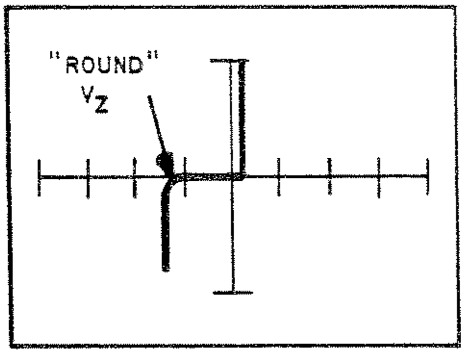


Figure 3-25. Signature of an Inferior Zener Diode in the Medium 1 Range at 60Hz

Figure 3-26 shows the connection of the base-emitter junction of an NPN transistor to the Tracker 2000. Figure 3-27 shows that the base-emitter junction of a silicon bipolar transistor (a PN2222) exhibits the property of a zener diode. The zener voltage (V_Z) can be determined from the signature. In this example, V_Z is approximately 6.3 Volts.

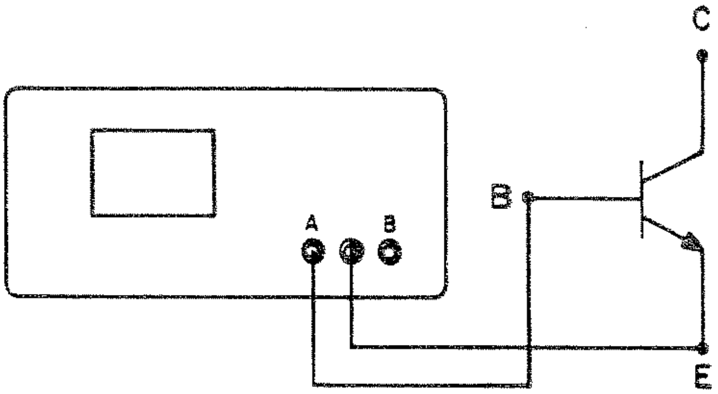


Figure 3-26. NPN Base-Emitter Junction Connections

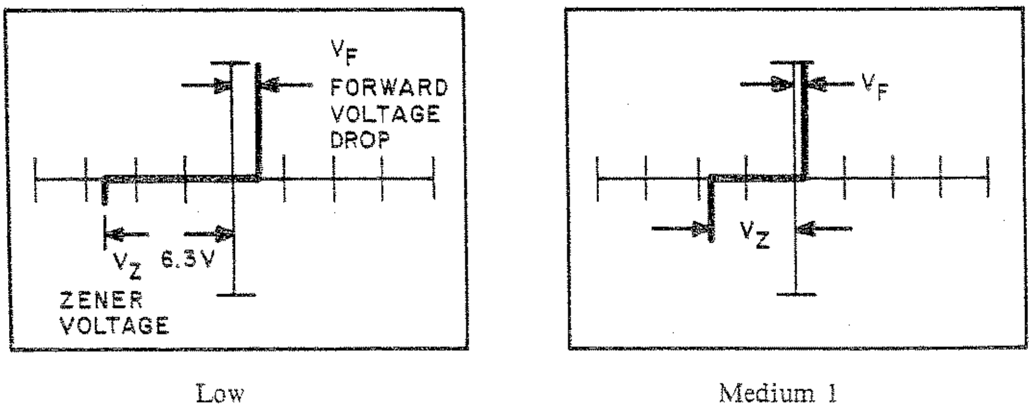
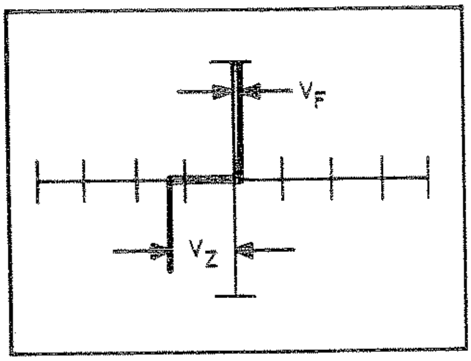
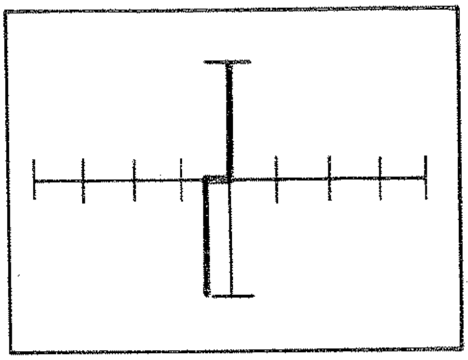


Figure 3-27a. Signatures of a PN2222 B-E Junction in the Low and Medium 1 Ranges at 60Hz



Medium 2



High

Figure 3-27b. Signatures of a PN2222 B-E Junction in the Medium 2 and High Ranges at 60Hz

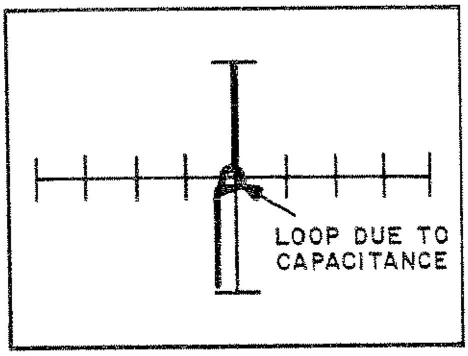


Figure 3-27c. Signature of a PN2222 B-E Junction in High Range at 2KHz

SECTION 4
TESTING TRANSISTORS

4.1 BIPOLAR JUNCTION TRANSISTORS

A bipolar junction transistor consists of a silicon crystal in which a layer of N-type silicon is sandwiched between two layers of P-type silicon. This type of transistor is referred to as a PNP type. Figure 4-1 shows a PNP and its circuit symbol.

A transistor may also consist of a layer of P-type silicon sandwiched between two layers of N-type silicon. This is referred to as an NPN transistor. Figure 4-2 shows an NPN transistor and its circuit symbol.

The three portions of a transistor are known as the emitter, base, and collector. The arrow on the emitter lead specifies the direction of current flow when the base-emitter is biased in the forward direction.

Figure 4-1. PNP Transistor and Circuit Symbol

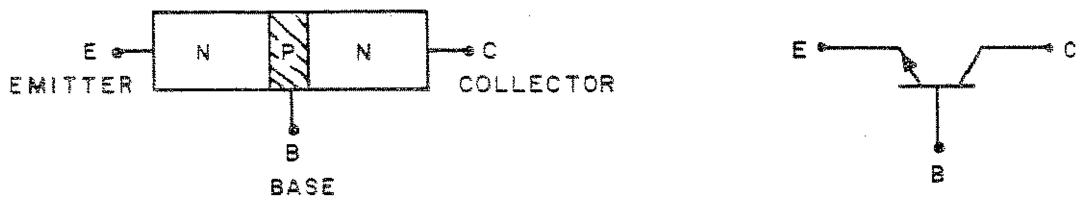
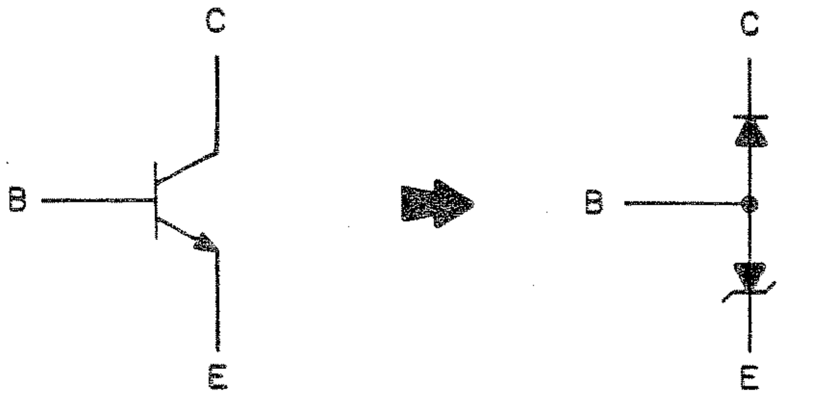


Figure 4-2. NPN Transistor and Circuit Symbol

The test signals at the Tracker 2000 probes are sinusoidal and can be used to forward bias, as well as reverse bias, a semiconductor junction. To test a transistor, the base-emitter (B-E), collector-base (C-B), and collector-emitter (C-E) junctions all need to be examined.

4.2 NPN BIPOLAR TRANSISTORS

A bipolar transistor consists of two PN junctions which the Tracker 2000 can examine in a manner similar to that used for testing diodes. Figure 4-3 shows an equivalent circuit for an NPN bipolar transistor.



Symbol

Equivalent Circuit

Figure 4-3. NPN Transistor

4.2.1 B-E Junction

To test the B-E junction, the test circuit in Figure 4-4 should be used. The B-E junction exhibits a zener diode characteristic, i.e. normal diode voltage drop under forward bias, and zener breakdown under reverse bias with V_Z usually in the range of 6 to 10 Volts. Figure 4-5 shows the signatures produced by the B-E junction of a 2N3904 NPN transistor in each range.

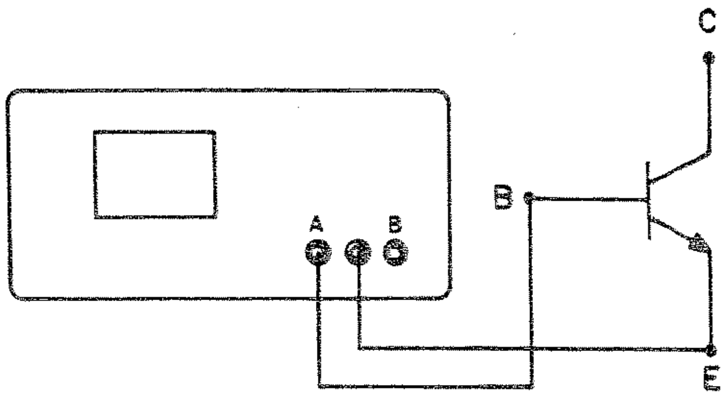


Figure 4-4. Base-Emitter Test Connections

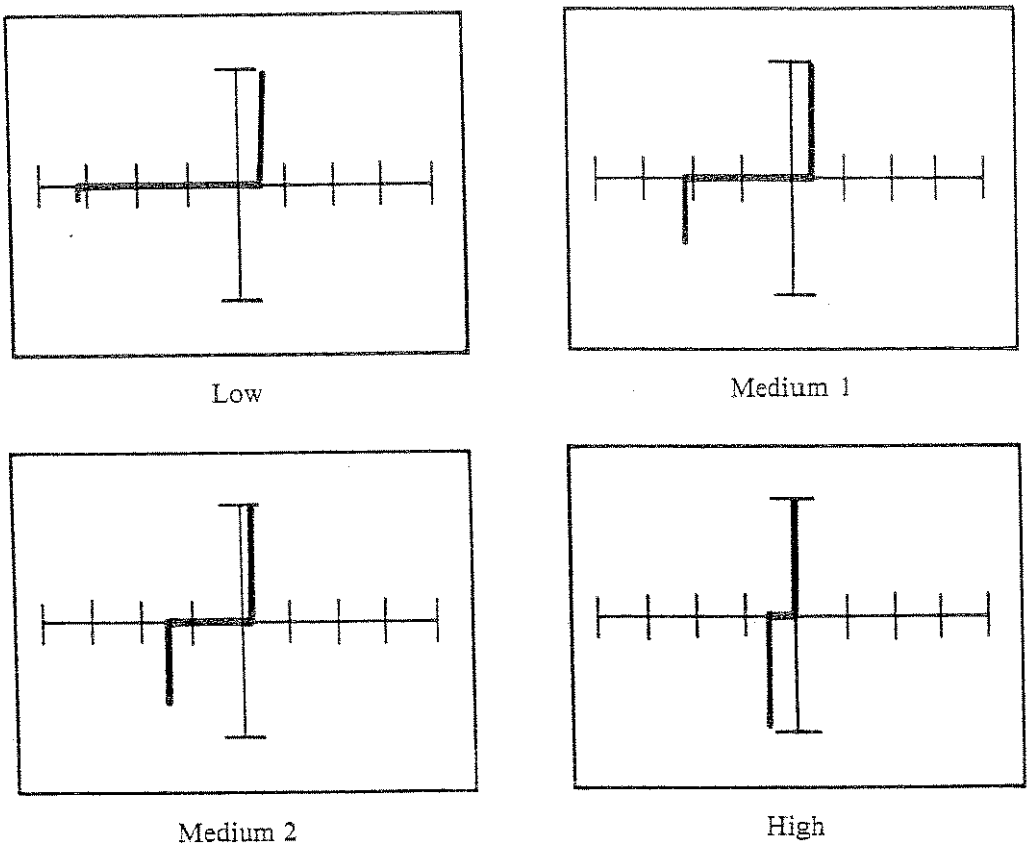


Figure 4-5. B-E Signatures of an NPN Transistor (2N3904) at 60Hz

4.2.2 C-E Connection

The test circuit for the C-E junction is shown in Figure 4-6. Referring to Figure 4-3, this test examines a series connection of the two junctions, i.e. a simple diode in series with a zener diode. The resulting signatures are shown in Figure 4-7. When the collector is positive with respect to the emitter (right side of display) the C-B diode is reverse biased and the combination appears as an open circuit. This is expected because the normal operation of an NPN transistor uses positive C-E voltage and there is no base drive in the test circuit. When the collector is negative with respect to the emitter, the C-B diode is forward biased and the B-E junction goes into zener breakdown. The low impedance section of the signature is displaced to the left of the vertical axis by the sum of the voltage drops across the two junctions.

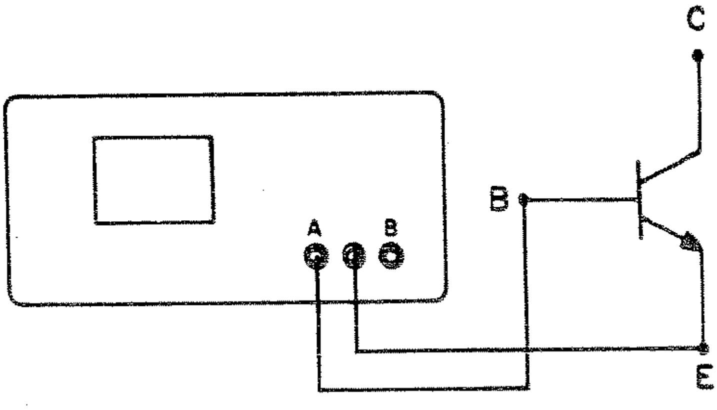


Figure 4-6. Collector-Emitter Test Connections

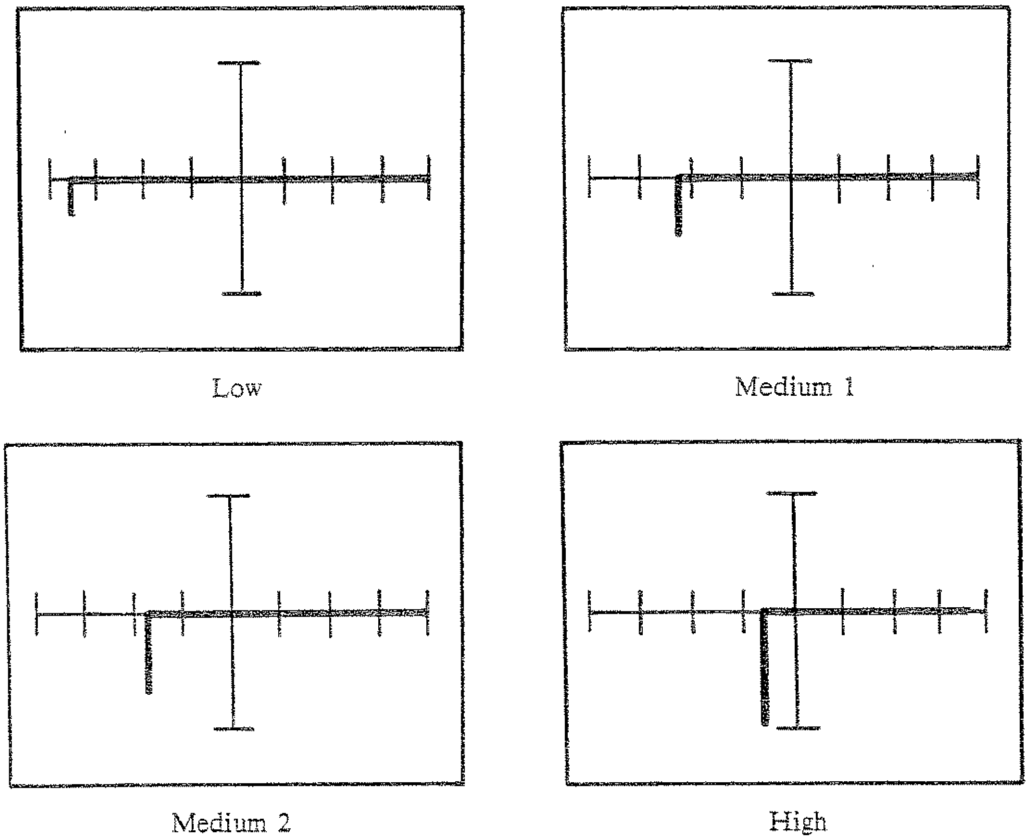


Figure 4-7. C-E Signatures of an NPN Transistor (2N3904) at 60Hz

4.2.3 C-B Junction

The C-B junction can be examined using the test circuit shown in Figure 4-8. From Figure 4-3, it is seen that this junction is a simple diode and it produces signatures like that of a diode in all ranges (Refer to Figure 4-9).

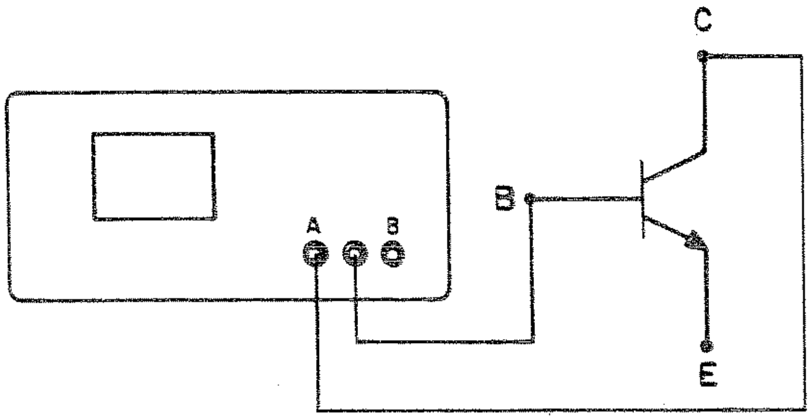


Figure 4-8. Collector-Base Test Connections

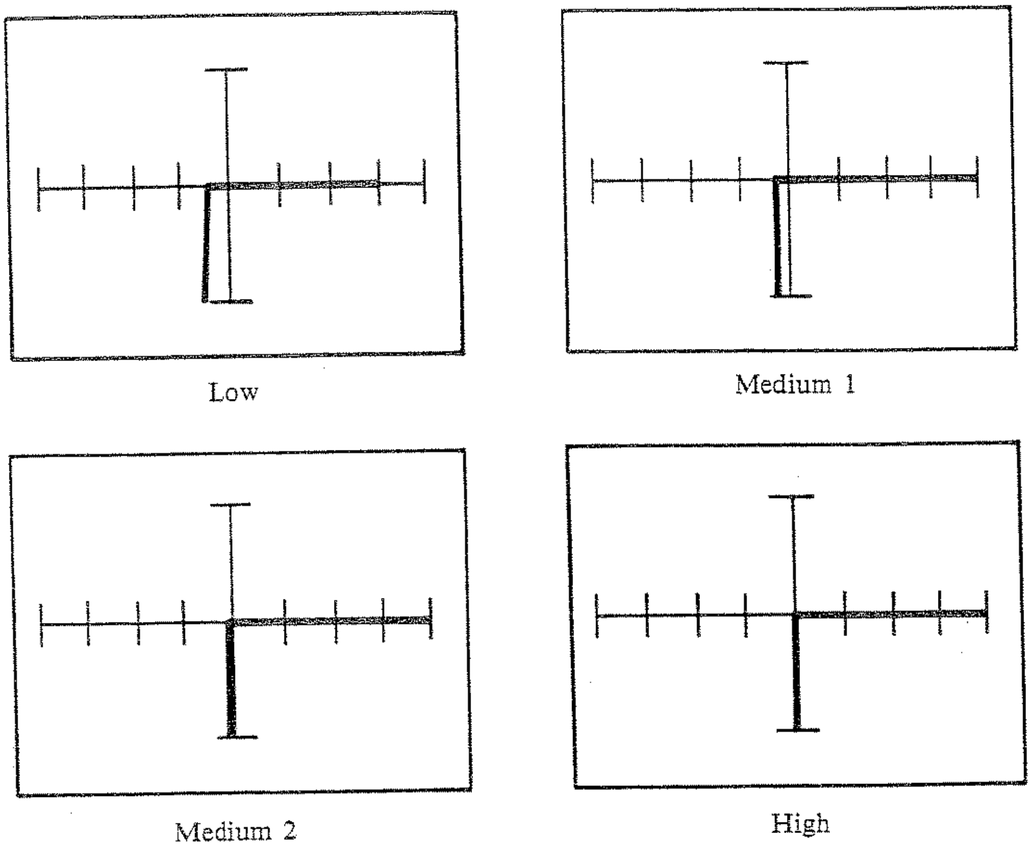


Figure 4-9. C-B Signatures of an NPN Transistor (2N3904) at 60Hz

4.3 PNP BIPOLAR TRANSISTORS

The testing of PNP transistors is the same as that described for NPN transistors, except that the signatures are reversed from those of an NPN device. This is because in the equivalent circuit of a PNP transistor, the polarity of the two diodes is reversed (see Figure 4-10).

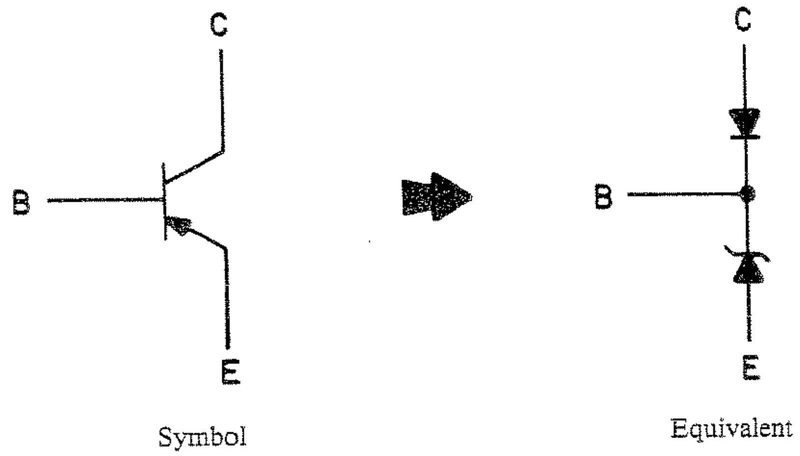


Figure 4-10. PNP Transistor

4.3.1 B-E Junction

To test the B-E junction, the test circuit of Figure 4-11 is used, and the signatures are shown in Figure 4-12.

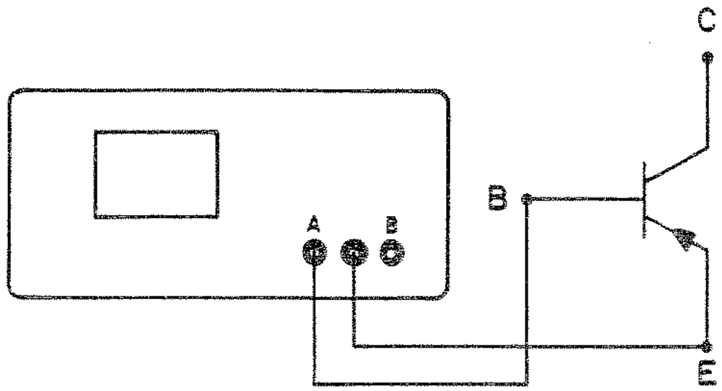


Figure 4-11. Base-Emitter Test Connections

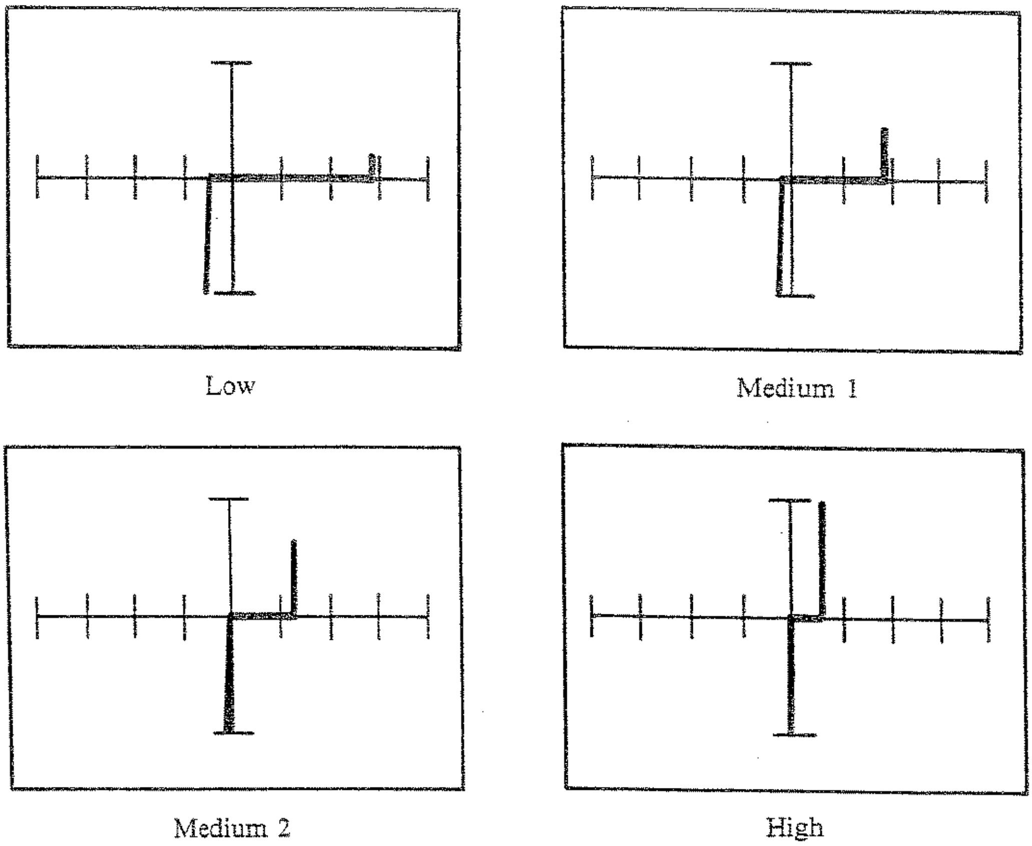


Figure 4-12. B-E Signatures of a PNP Transistor (2N3906) at 60Hz

4.3.2 C-E Connection

The test circuit is shown in Figure 4-13 and the signatures are shown in Figure 4-14.

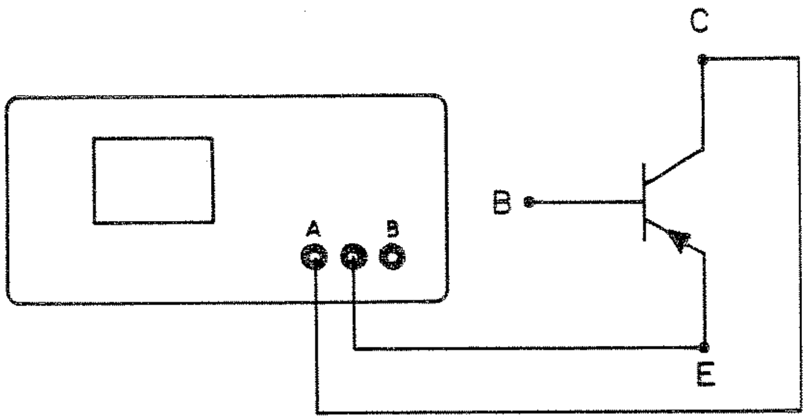


Figure 4-13. Collector-Emitter Test Connections

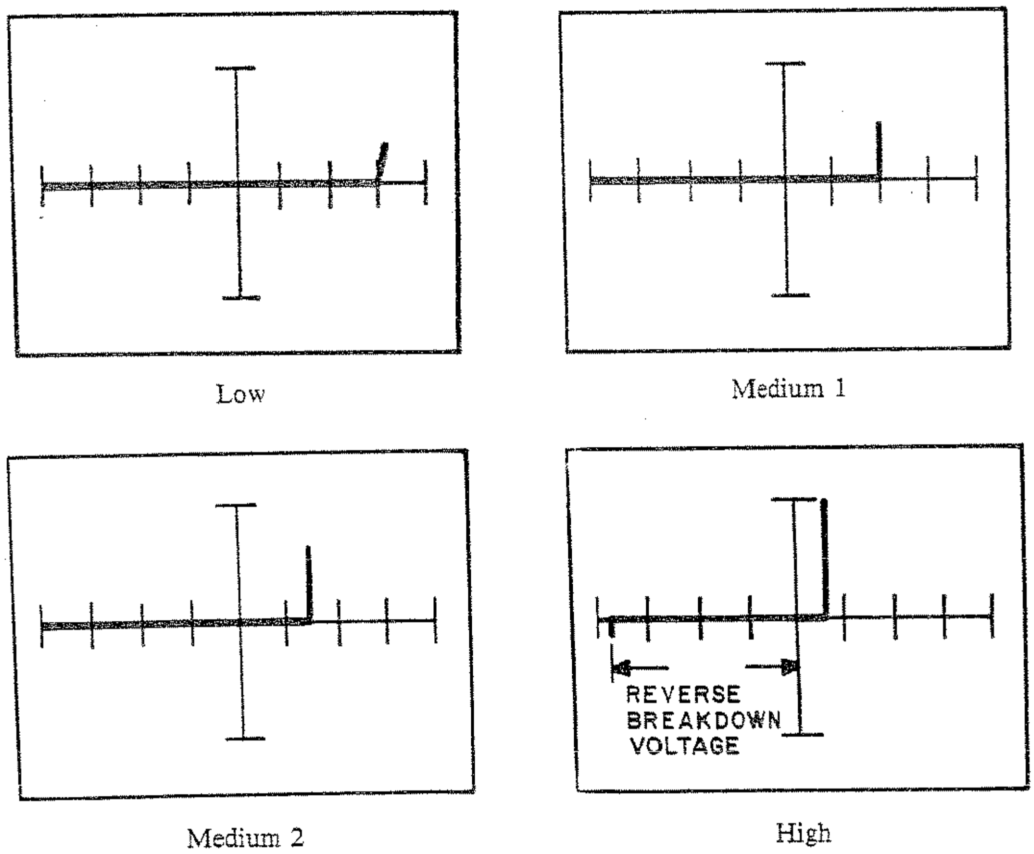


Figure 4-14. C-E Signatures of a PNP Transistor (2N3906) at 60Hz

4.3.3 C-B Junction

The test circuit is shown in Figure 4-15 and the signatures are shown in Figure 4-16.

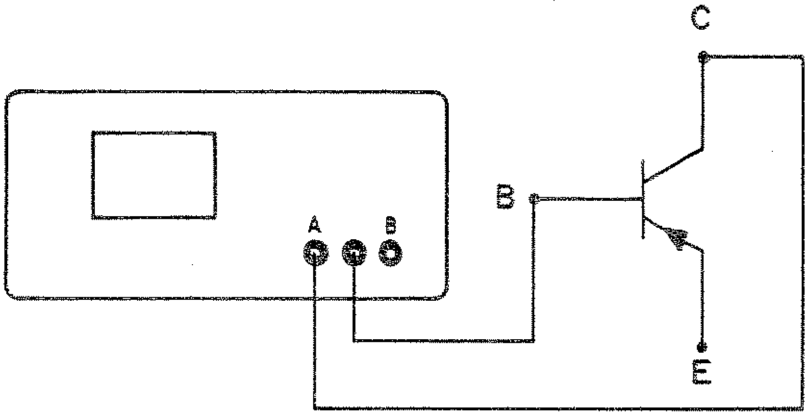


Figure 4-15. Collector-Base Test Connections

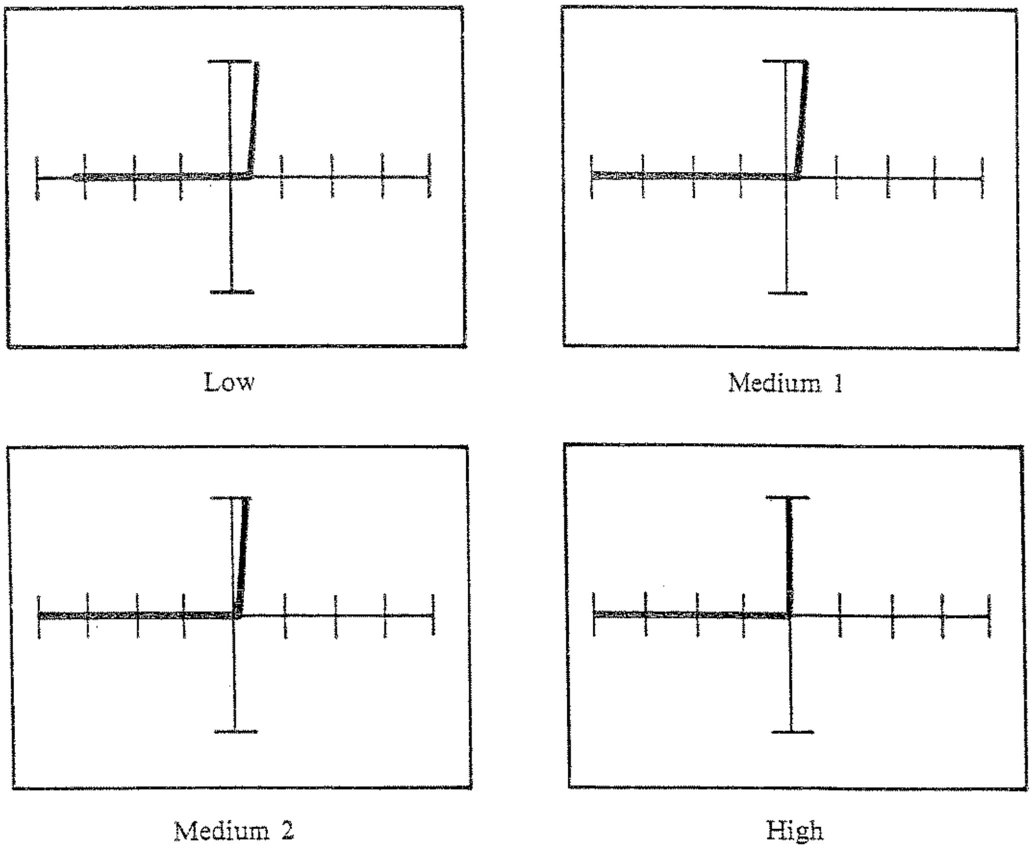
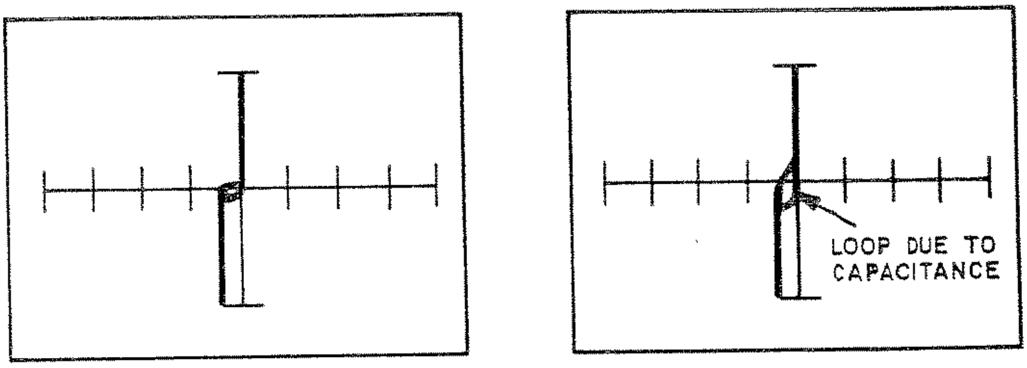


Figure 4-16. C-B Signatures of a PNP Transistor (2N3906) at 60Hz

4.4 POWER TRANSISTORS — NPN AND PNP

Transistor testing procedures described in sections 4-3 and 4-4 are applicable to power transistors. However, most power transistors show capacitance in the signature when the high range is used. Figure 4-17 shows the loop in the signature caused by capacitance.



High 60Hz

High 2KHz

Figure 4-17. B-E Signatures of a Power Transistor (TIP50) at 60Hz and 2KHz

4.5 DARLINGTON TRANSISTORS

The Darlington transistor is basically two transistors connected to form a composite pair as shown in Figure 4-18. The input resistance of Q2 constitutes the emitter load for Q1.

Darlington transistors are tested in the same manner as NPN and PNP bipolar transistors, except that their signatures differ. Figure 4-19 shows the equivalent circuit of a commonly used Darlington transistor, the TIP112, and its pin assignments.

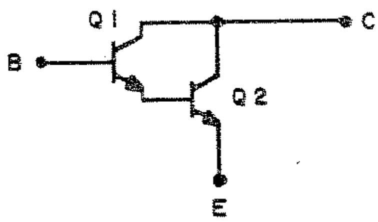


Figure 4-18. Darlington Transistor — Schematic Diagram

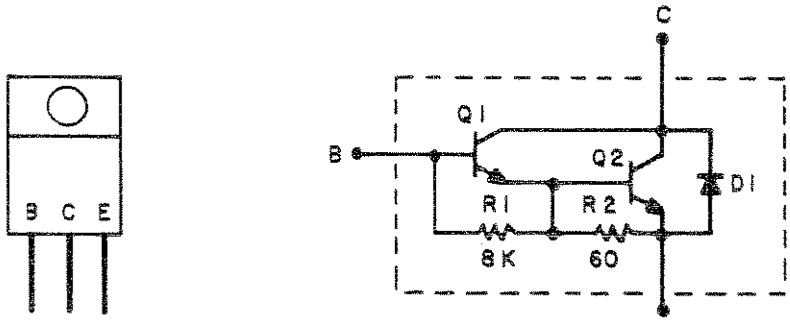


Figure 4-19. The TIP112 Darlington Transistor

4.5.1 Comparing B-E Junctions

It is useful to compare the B-E junction of a Darlington transistor with that of a regular transistor. Figure 4-20 shows the test connections and Figure 4-21 shows the signatures.

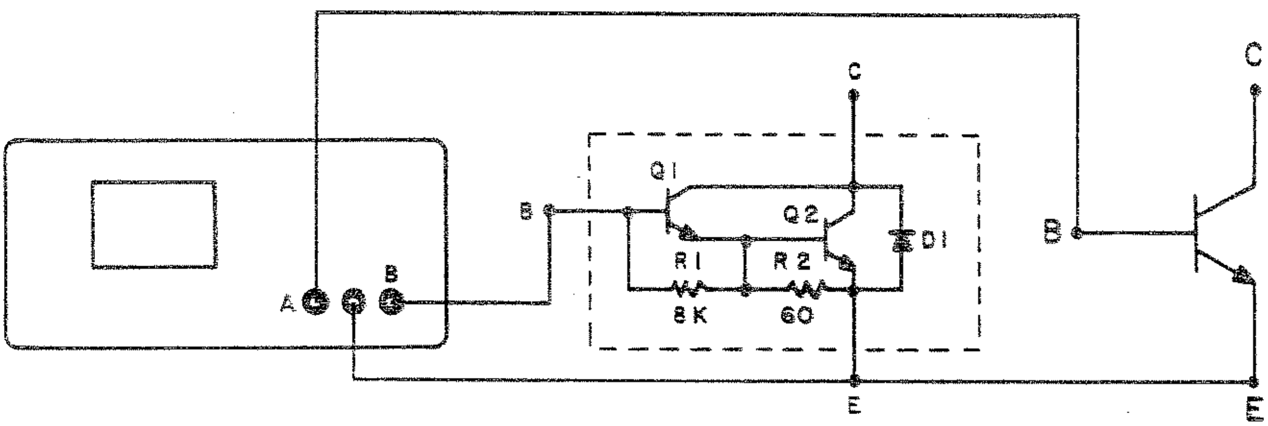


Figure 4-20. Base-Emitter Test Connections

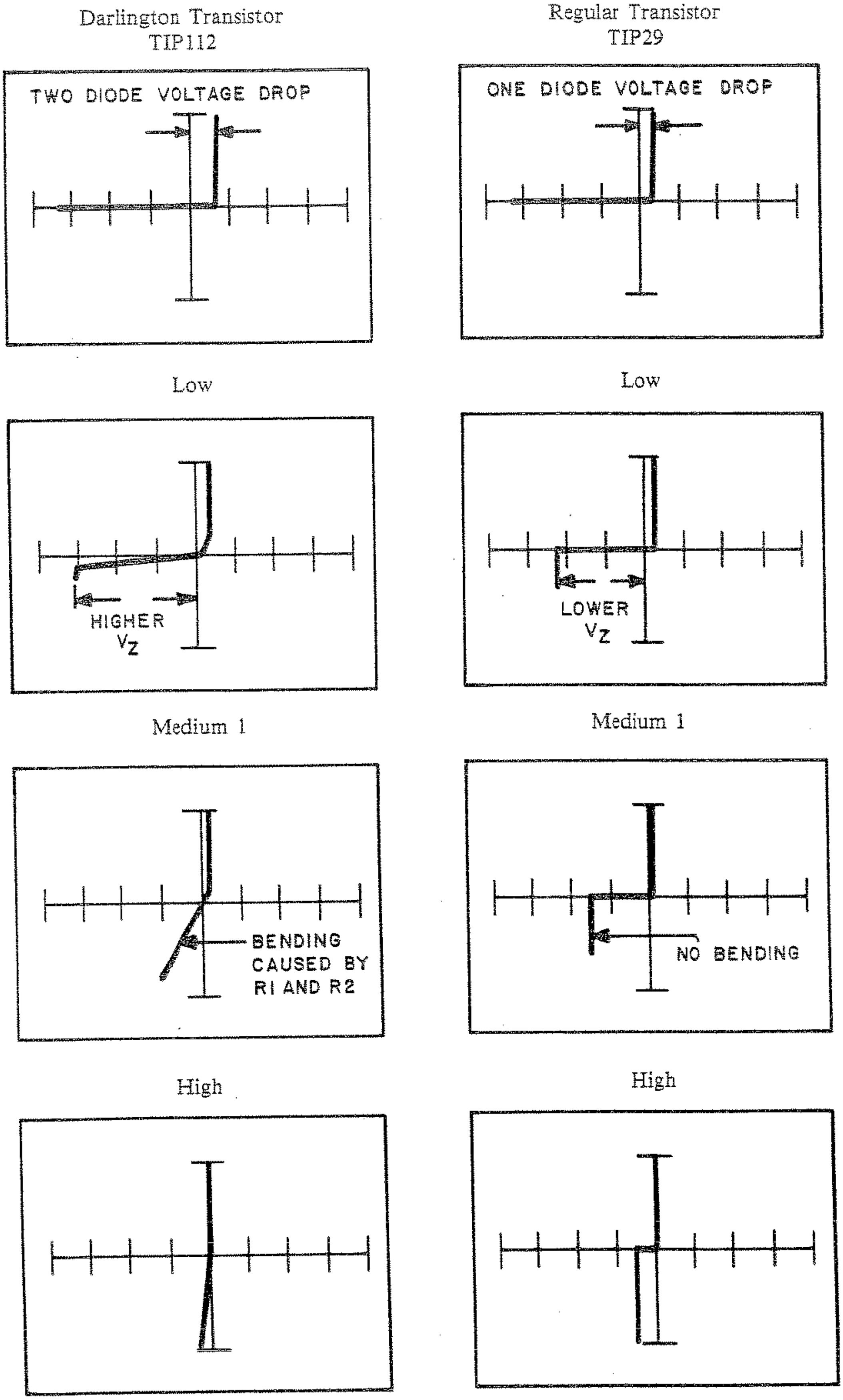


Figure 4-21. B-E Signature Comparison of a Darlington Transistor (TIP112) and a Regular Transistor (TIP29) at 60Hz.

4.5.2 Comparing C-E Connections

This section compares the C-E junctions of a Darlington transistor and a regular transistor. Figure 4-22 shows the test circuit and Figure 4-23 shows the signatures.

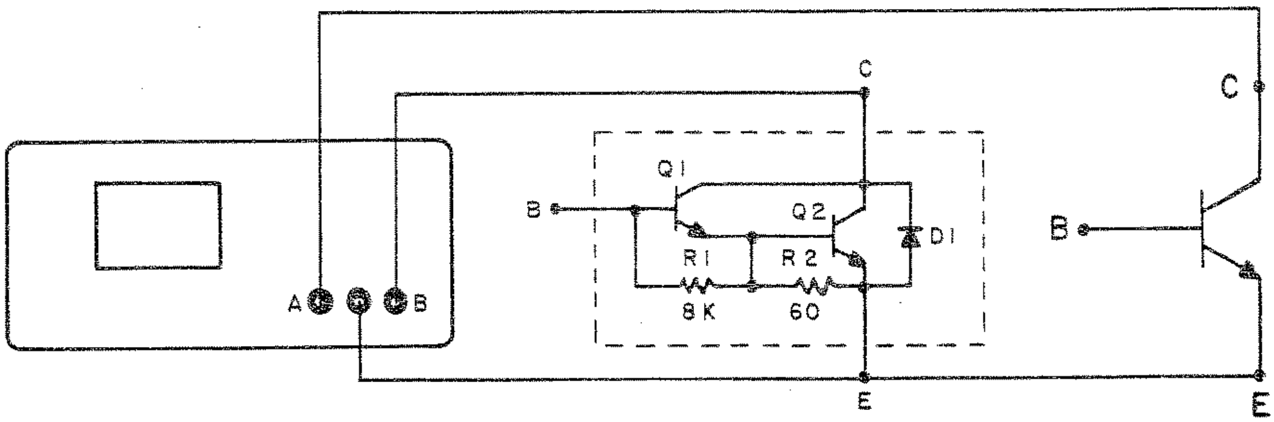


Figure 4-22. Collector-Emitter Test Connections

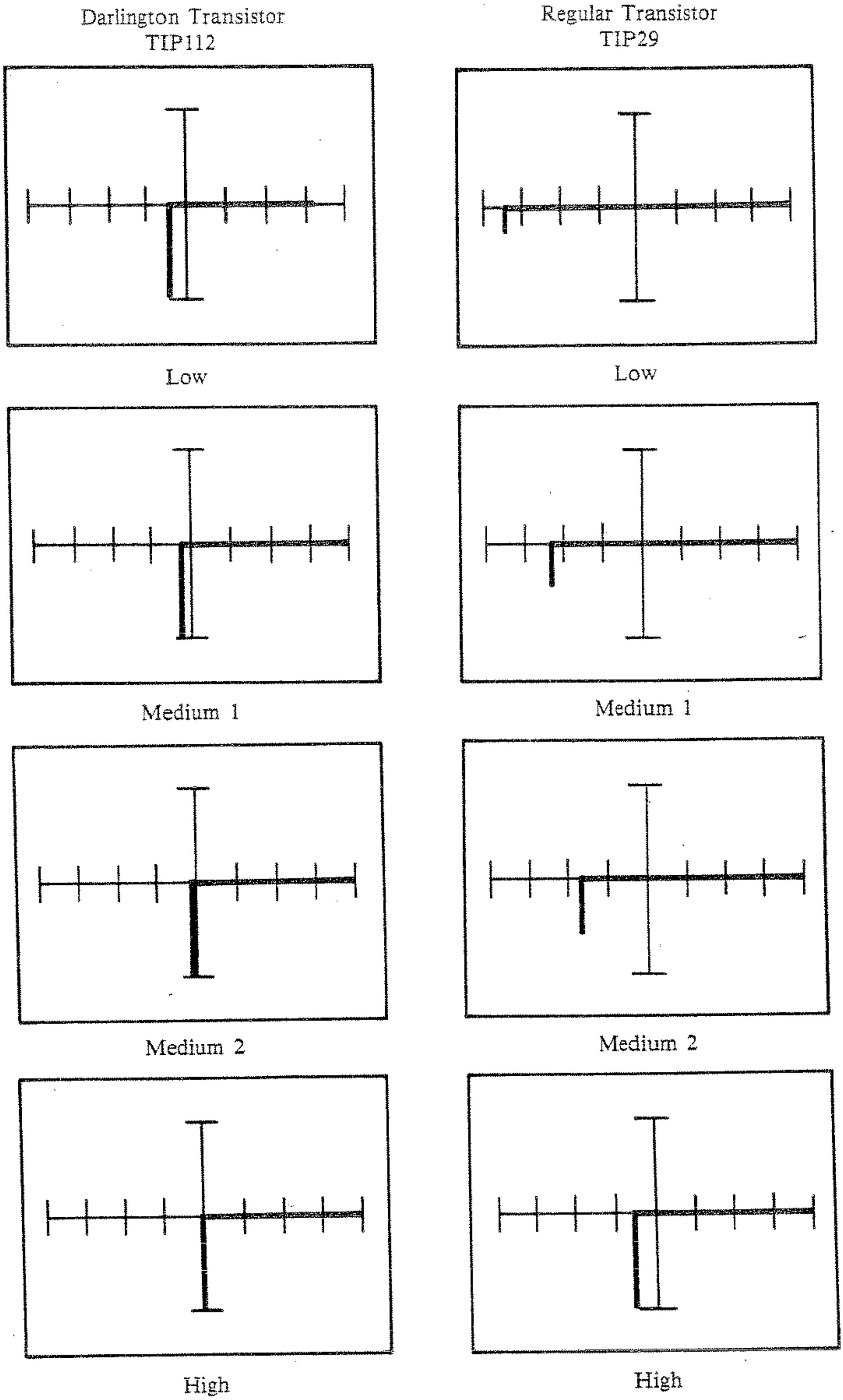


Figure 4-23. C-E Signature Comparison of a Darlington Transistor (TIP112) and a Regular Transistor (TIP29) at 60Hz

4.5.3 Comparing C-B Junctions

The C-B signatures of a Darlington transistor are the same as the C-E signatures. They are also the same as the C-B signatures of a regular transistor.

4.6 JUNCTION FIELD EFFECT TRANSISTORS

The structure of an N-channel Junction Field Effect Transistor (JFET) is shown in Figure 4-24. Resistive contacts are made to the ends of a semiconductor bar of N-type material (if P-type material is used, the device is referred to as a P-channel JFET). The voltage supply connected to the ends causes current to flow along the length of the bar. This current is made up of majority carriers, which in this case are electrons. The circuit symbol is shown in Figure 4-25. The following FET notation is standard.

SOURCE: The source (S) is the terminal at which the majority carriers enter the bar. The current entering the bar at S is designated by I_s.

DRAIN: The drain (D) is the terminal at which the majority carriers leave the bar. The current entering the bar at D is designated by I_d. If D is more positive than S then the drain to source voltage (D_{ds}) is positive.

GATE: On both sides of the N-type bar shown in Figure 4-24, heavily doped (P +) sections of acceptor impurities have been created by alloying, by diffusion, or by some other means of creating P-N junctions. These sections of impurities are called the gate (G). The gate to source voltage (V_{gs}) is applied to reverse bias the P-N junction. The current entering the bar is designated I_g.

CHANNEL: The section of N-type material between the two gate sections is the channel through which the majority carriers travel from source to drain.

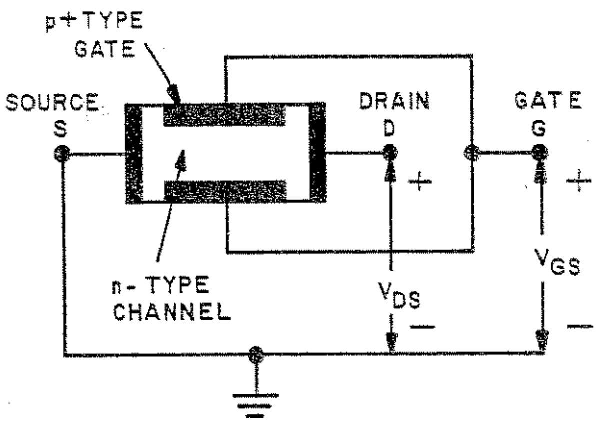


Figure 4-24. The Basic Structure of an N-Channel Junction Field Effect Transistor.

NOTE: In a P-channel JFET the voltages would be reversed.

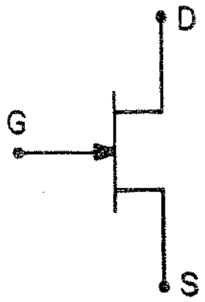


Figure 4-25. Circuit Symbol for an N-Channel JFET

Figure 4-26 shows the pin connections of an N-channel JFET (2N5638).

Figure 4-26. N-Channel JFET (2N5638) Pin Connections, Bottom View

4.6.1 Drain-Source Connection

Figure 4-27 shows the drain-source (D-S) test circuit and Figure 4-28 shows the signatures in each range.

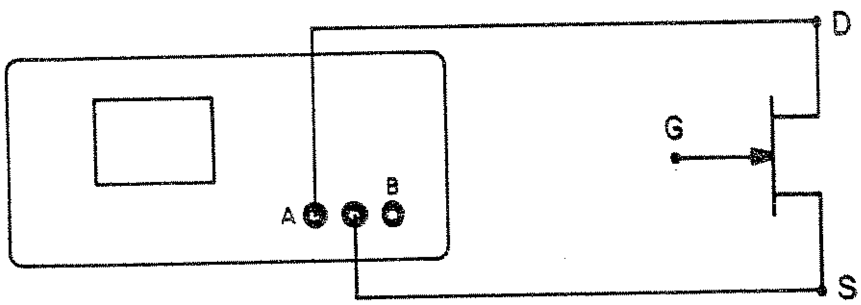


Figure 4-27. Drain-Source Test Connection

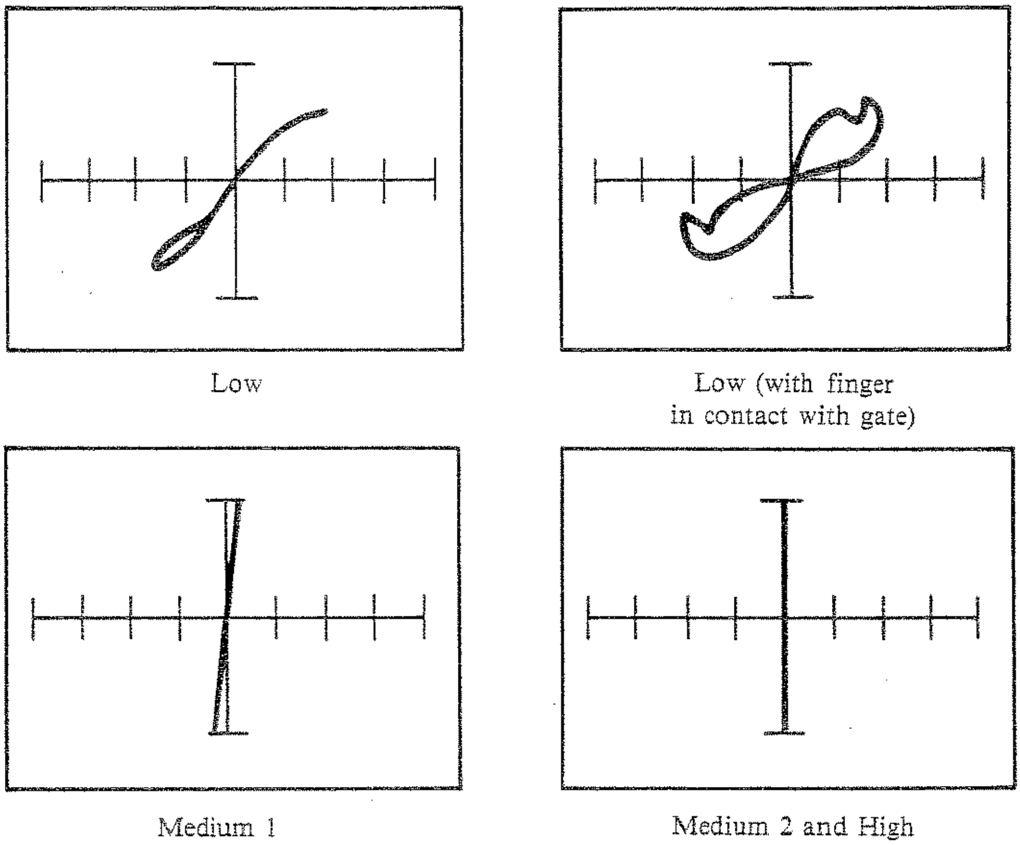


Figure 4-28. D-S Signatures of an N-Channel JFET (2N5638) at 60Hz

4.6.2 Gate-Drain Connection

Figure 4-29 shows the gate-drain (G-D) test circuit and figure 4-30 shows the signatures.

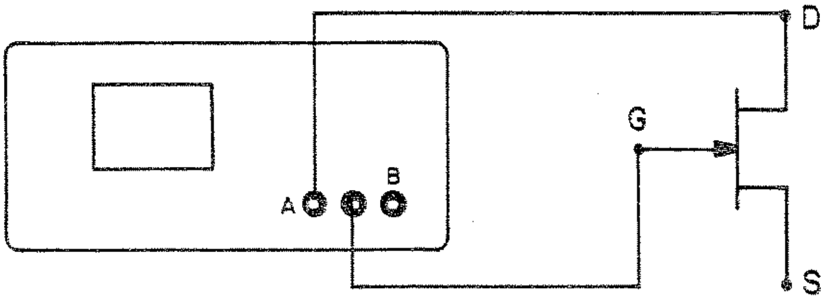


Figure 4-29. Gate-Drain Test Circuit

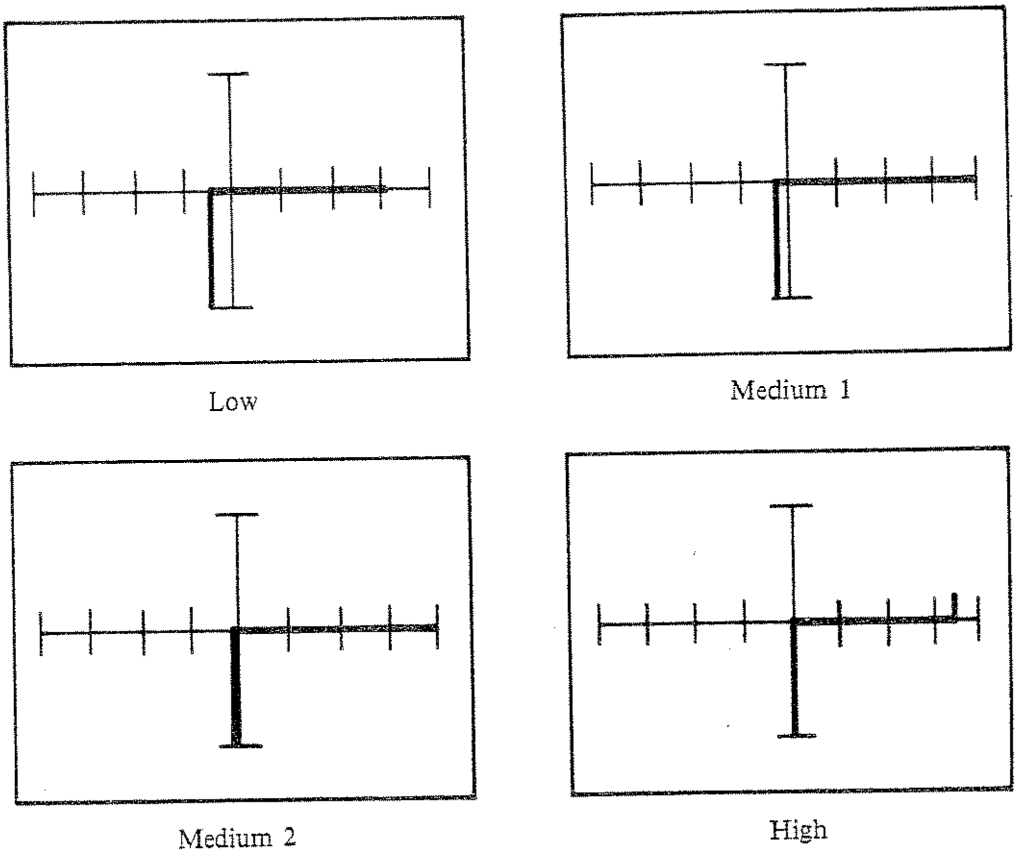


Figure 4-30. G-D Signatures of an N-Channel JFET (2N5638) at 60Hz

4.6.3 Source-Gate Connection

Figure 4-31 shows the source-gate (S-G) test circuit and figure 4-32 shows the signatures.

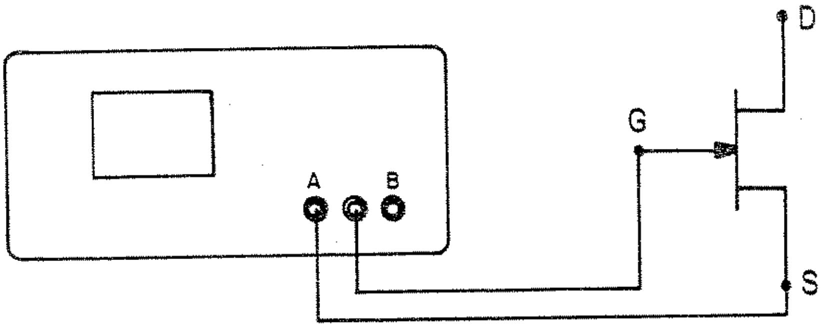


Figure 4-31. Source-Gate Test Circuit

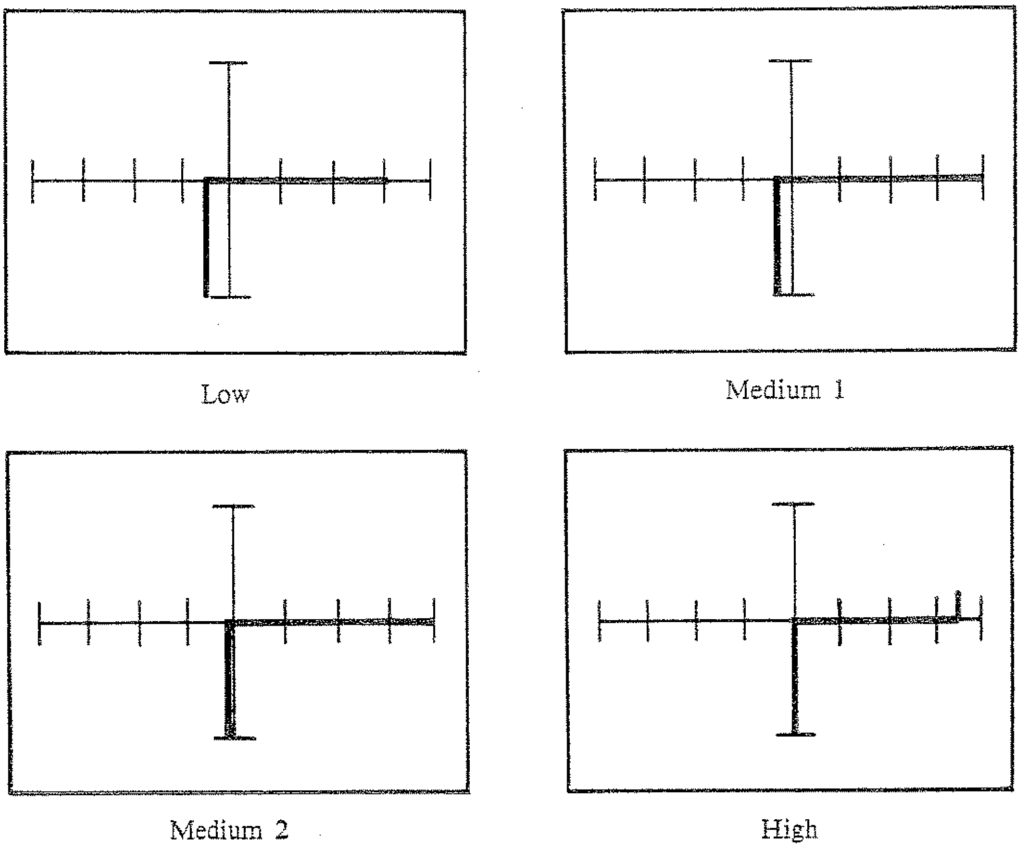
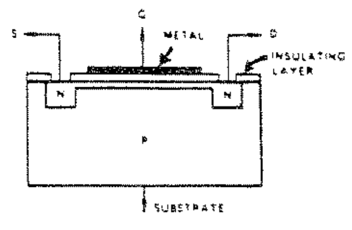


Figure 4-32. S-G Signatures of an N-Channel JFET (2N5638) at 60Hz

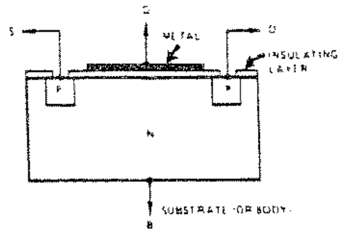
4.7 MOS FIELD TRANSISTORS

MOS field effect transistors (MOSFETs) are constructed as either "depletion" or "enhancement" mode devices. Each type requires a distinct test procedure with the Tracker 2000. Figure 4-33 shows the construction and circuit symbol of N-channel and P-channel MOSFETs. The depletion mode MOSFET is a "normally on" device. When $V_{gs} = 0$, a conducting path exists between source and drain. An enhancement mode MOSFET is a "normally off" device, and increasing the voltage applied to the gate will enhance channel conduction, and depletion will never occur.

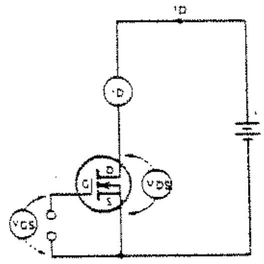
Because MOS devices require higher voltage levels for testing than JFETs, the medium 2 range must be used. The amount of "in circuit" loading that can be tolerated is limited by the impedance of the signal generator inside the Tracker 2000.



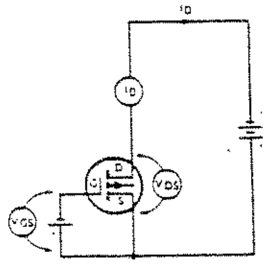
Idealized cross-section through an N-channel depletion-type MOSFET



Idealized cross-section through a P-channel enhancement MOSFET



Circuit arrangement for N-channel depletion MOSFET



Circuit arrangement for P-channel enhancement MOSFET

Figure 4-33. N-channel and P-channel MOSFET Devices

4.8 MOSFET WITH PROTECTION DIODE, VN10KM

Some MOSFET devices have an input protection diode, and the Tracker 2000 displays the effect of this diode. Figure 4-34 shows a Siliconix N-channel enhancement mode MOSFET (VN10KM). This device has a protection diode between the gate and source, and the substrate is internally connected to the source.

4.8.1 Source-Gate Connection

To test the gate and source of the VN10KM, connect the test probes to the gate (G) and source (S) terminals as shown in Figure 4-35. Note that the drain (D) terminal is not connected.

Figure 4-36 shows the signatures of the protection zener diode in the low, medium 1, medium 2 and high ranges. The test signal in the low range is 20 Volts peak to peak and is not high enough to cause zener breakdown. The test signal in the medium 2 range is 40 Volts peak to peak, and is just high enough to cause zener breakdown. However, in the high range, the test signal is sufficient to cause zener breakdown.

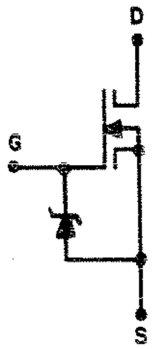


Figure 4-34. VN10KM MOSFET With a Source to Gate Protection Diode

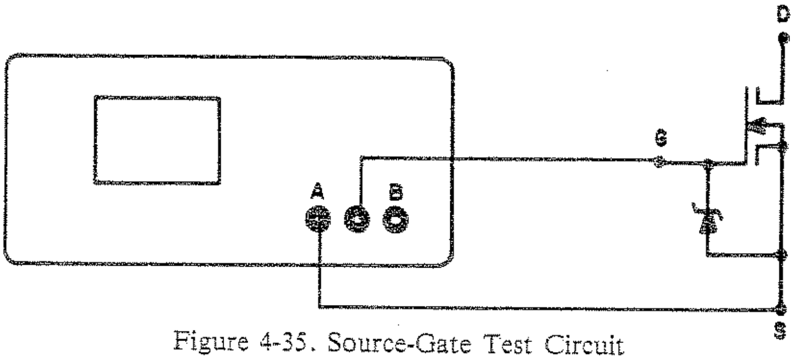
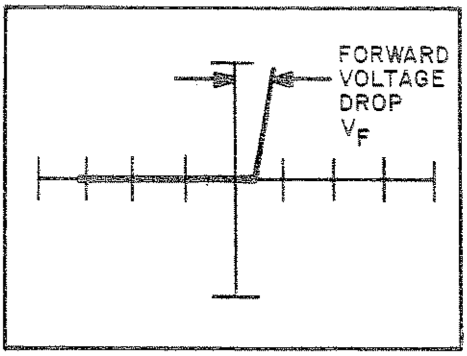
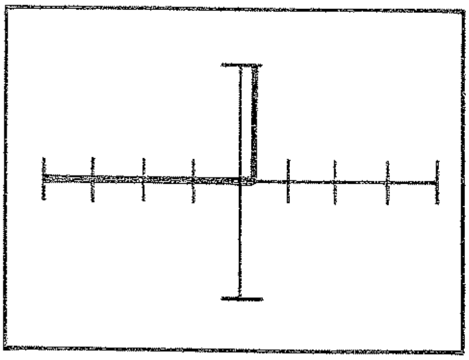


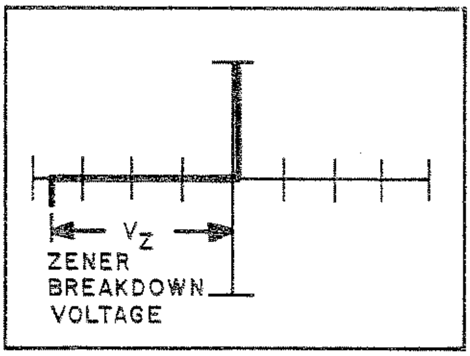
Figure 4-35. Source-Gate Test Circuit



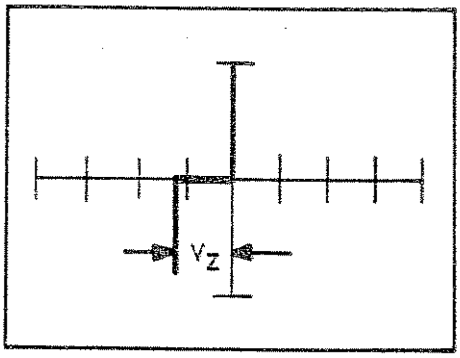
Low



Medium 1



Medium 2



High

Figure 4-36. S-G Signatures of an N-channel Enhancement Mode MOSFET (VN10KM) at 60Hz

4.8.2 Drain-Source Connection

Figure 4-37 shows the drain-source (D-S) test circuit and Figure 4-38 shows the signatures.

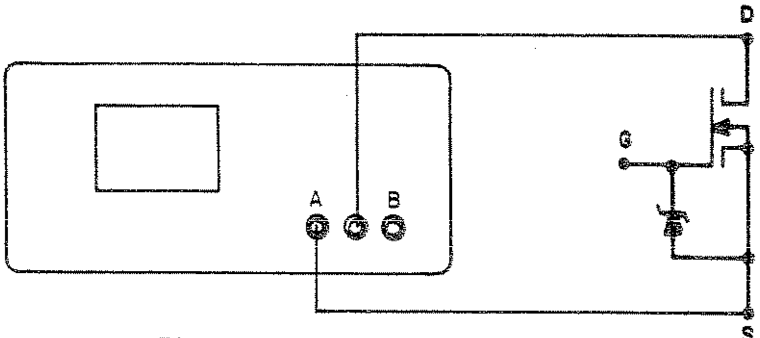


Figure 4-37. Drain-Source Test Circuit

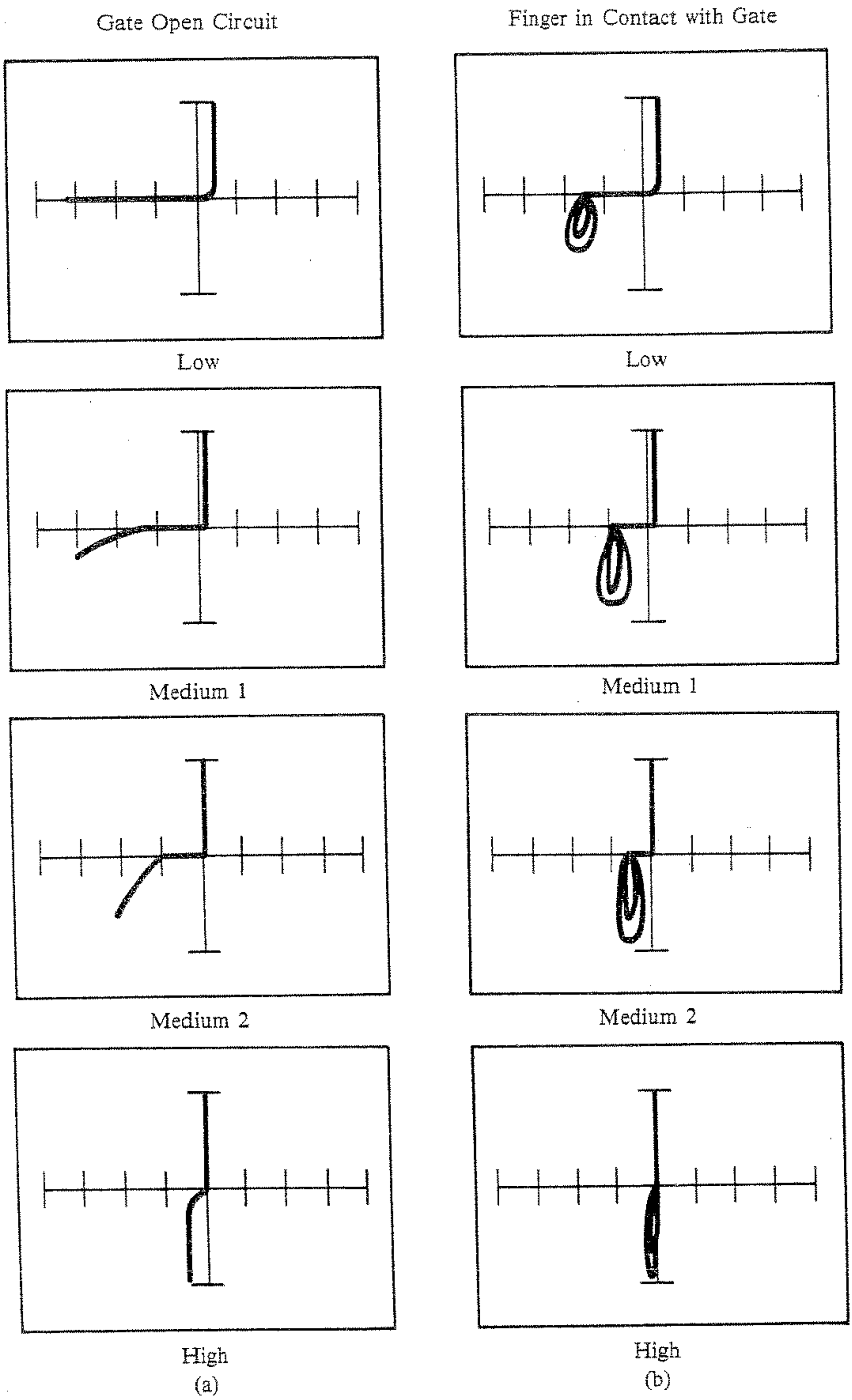


Figure 4-38. (a) Shows the D-S signatures of the MOSFET VN10KM when the gate is an open circuit while (b) shows the signatures when the user's finger is in contact with the gate, at 40Hz.

4.8.3 Gate-Drain Connection

Figure 4-39 shows the gate-drain (G-D) test circuit, and Figure 4-40 shows the signatures.

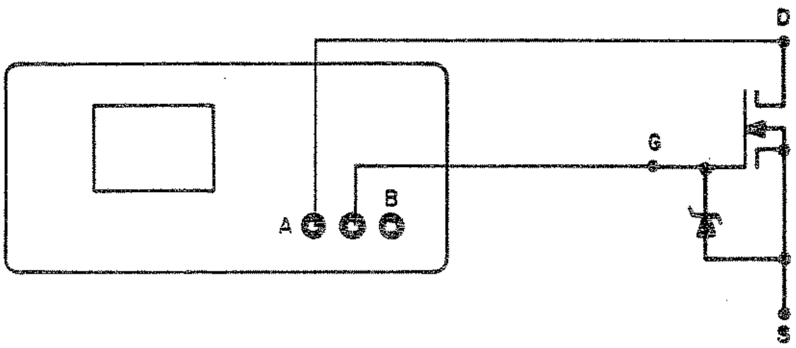


Figure 4-39. Gate-Drain Test Circuit

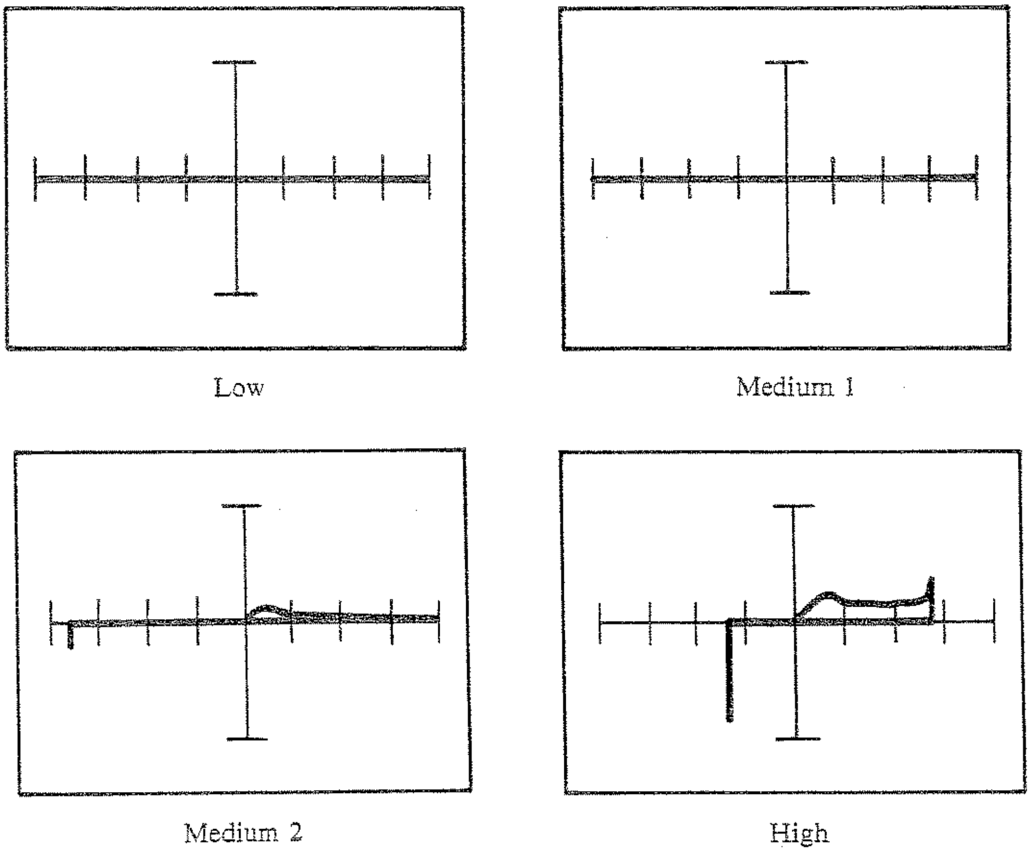


Figure 4-40. G-D Signatures of an N-channel Enhancement Mode MOSFET (VN10KM) at 60Hz

4.9 MOSFET WITHOUT A PROTECTION DIODE, VN10LM

Figure 4-41 shows a Siliconix N-channel enhancement mode MOSFET (VN10LM). This device does not have a protection diode between the gate and source, and the substance is internally connected to the source.

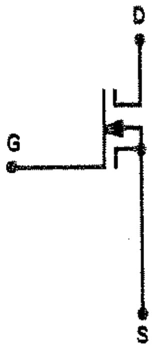


Figure 4-41. VN10LM MOSFET Without a Source to Gate Protection Diode

4.9.1 Source-Gate Connection

To test the gate and source of the VN10LM, connect the test probes to the gate (G) and source (S) terminals as shown in Figure 4-42. Note that the drain (D) terminal is not connected. Figure 4-43 shows the signatures.

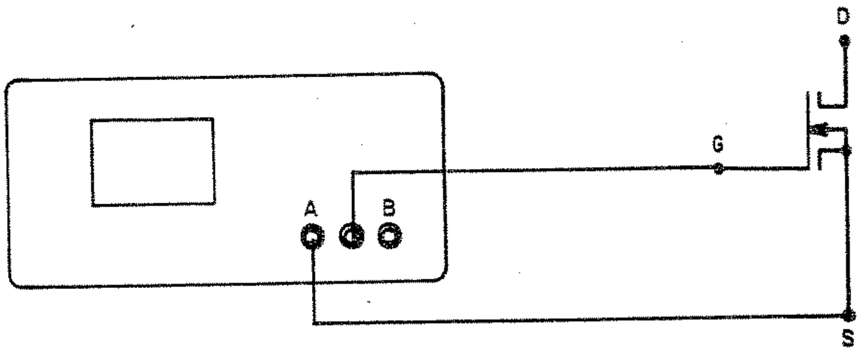


Figure 4-42. Source-Gate Test Circuit

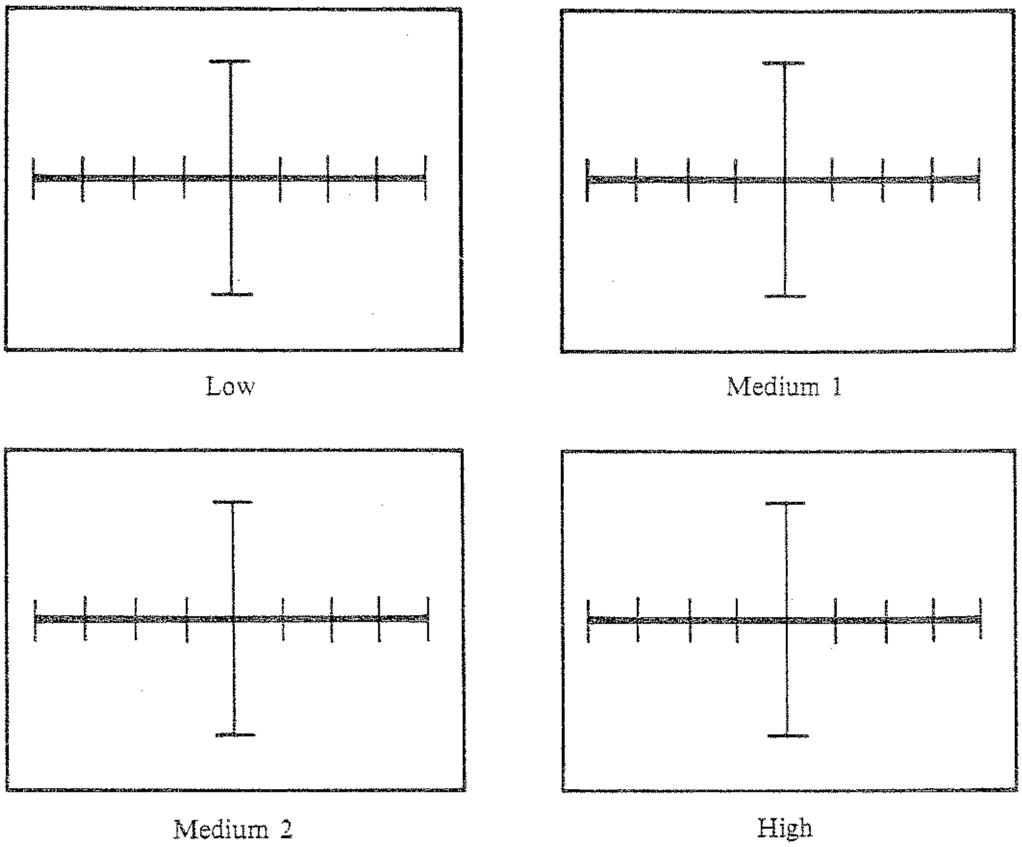


Figure 4-43. S-G Signatures of an N-channel Enhancement Mode MOSFET (VN10LM) at 60Hz

4.9.2 Drain-Source Connection

Figure 4-44 shows the drain-source (D-S) test circuit, and Figure 4-45 shows the signatures.

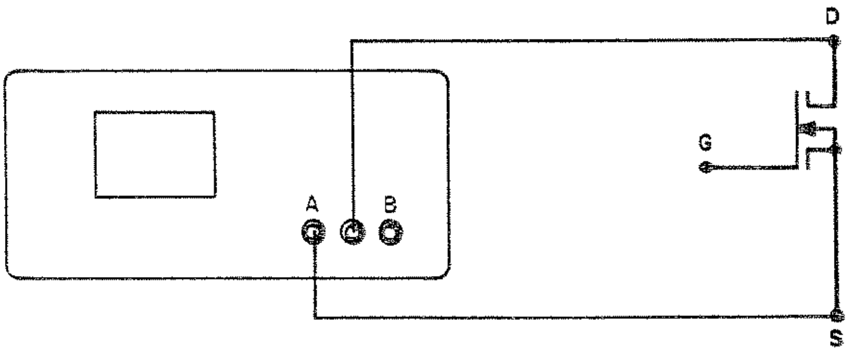


Figure 4-44. Drain-Source Test Circuit

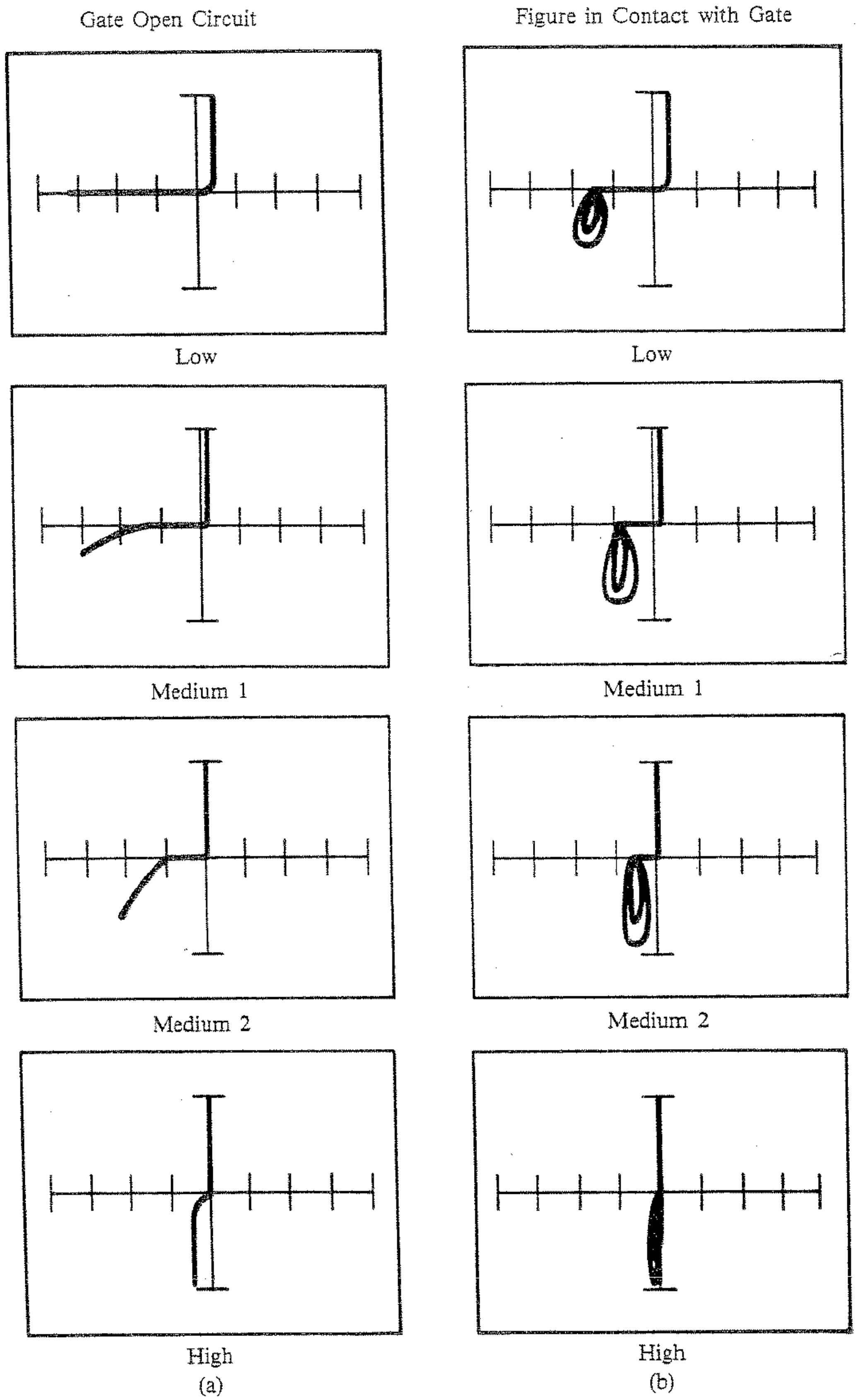


Figure 4-45. (a) shows the D-S signatures of the MOSFET VN10LM when the gate is an open circuit while (b) shows the signature when the user's finger is in contact with the gate, at 400Hz.

4.9.3 Gate-Drain Connection

Figure 4-46 shows the gate-drain (G-D) test circuit, and Figure 4-47 shows the signatures.

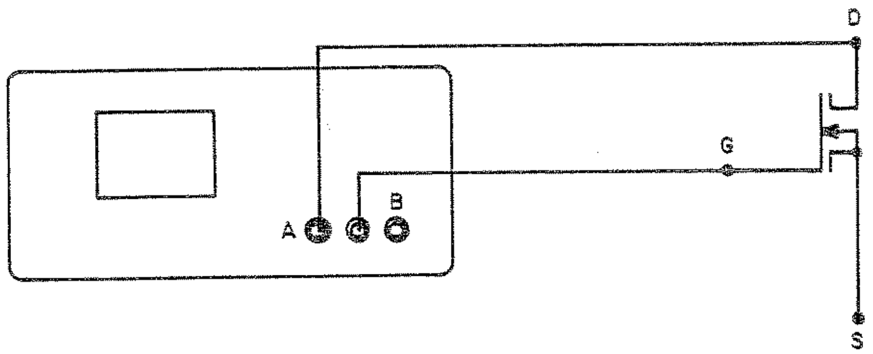


Figure 4-46. Gate-Drain Test Circuit

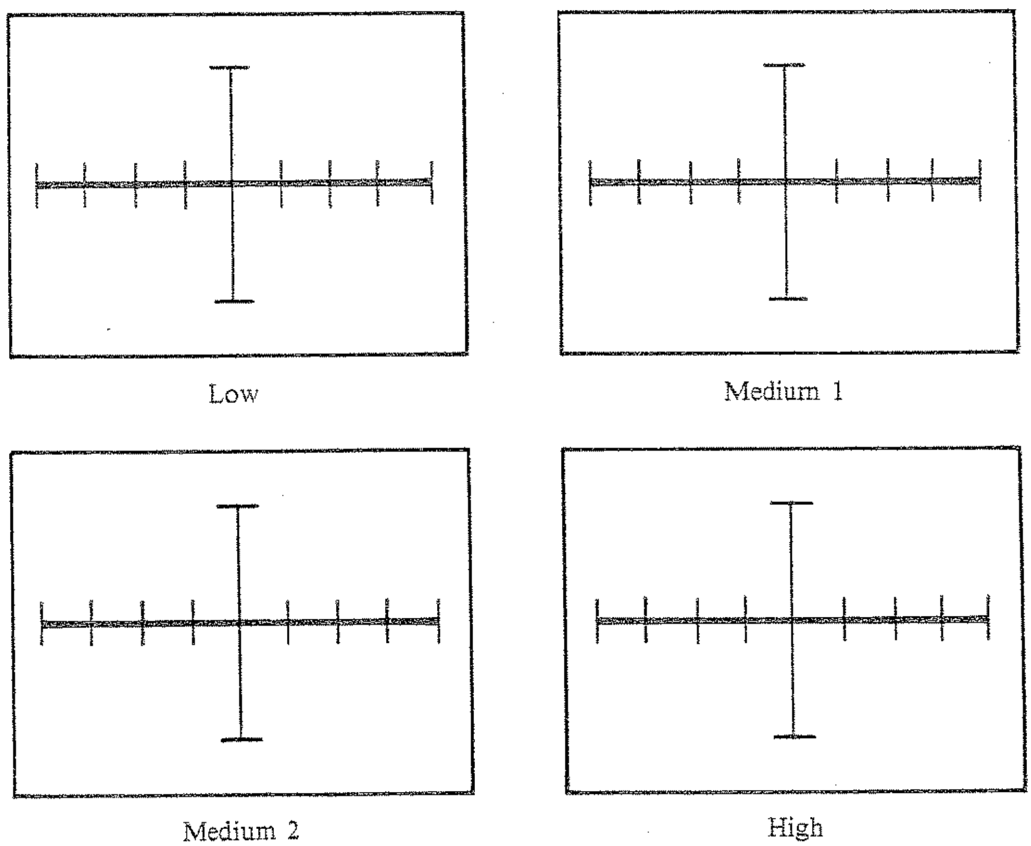


Figure 4-47. G-D Signatures of an Enhancement Mode MOSFET (VN10LM) at 60Hz

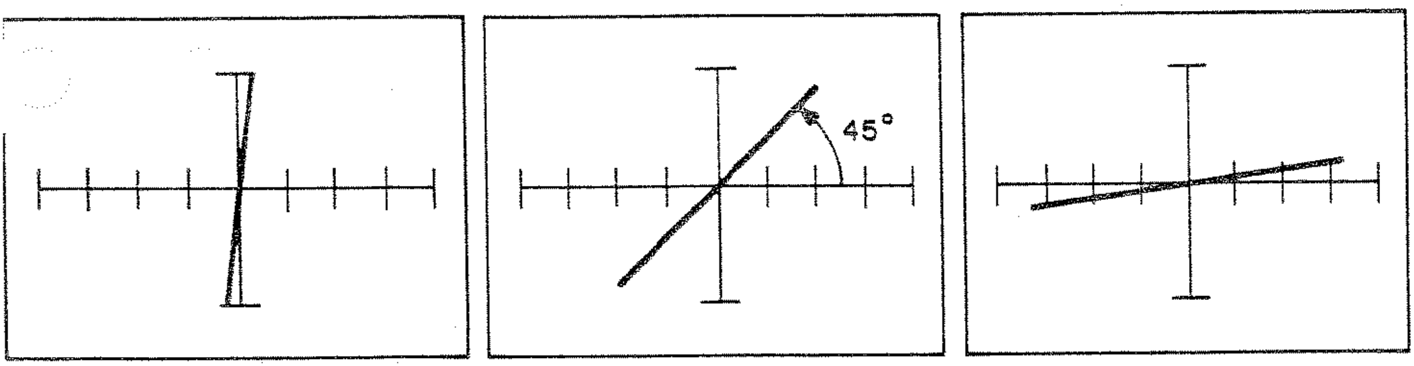
SECTION 5
RESISTORS, CAPACITORS, AND INDUCTORS

5.1 TESTING RESISTORS

A pure resistance across the test probes will cause the trace on the Tracker 2000 display to rotate in a counterclockwise direction around its center axis from an open circuit position. The degree of rotation is a function of the resistance value.

5.1.1 Low Range

The low range is designed to detect resistance between 1 ohm and 1K ohm. Figure 5-1 shows the effect of resistance on the angle of rotation in low range. A 1 ohm resistor causes almost 90 degrees of rotation, and a 50 ohm resistor produces a 45 degree rotation. A 400 ohm resistor causes a small rotation in angle. Resistors lower than 1 ohm appear as a short circuit (i.e. vertical trace) and resistance values above 400 ohms look like open circuits (i.e. horizontal trace).

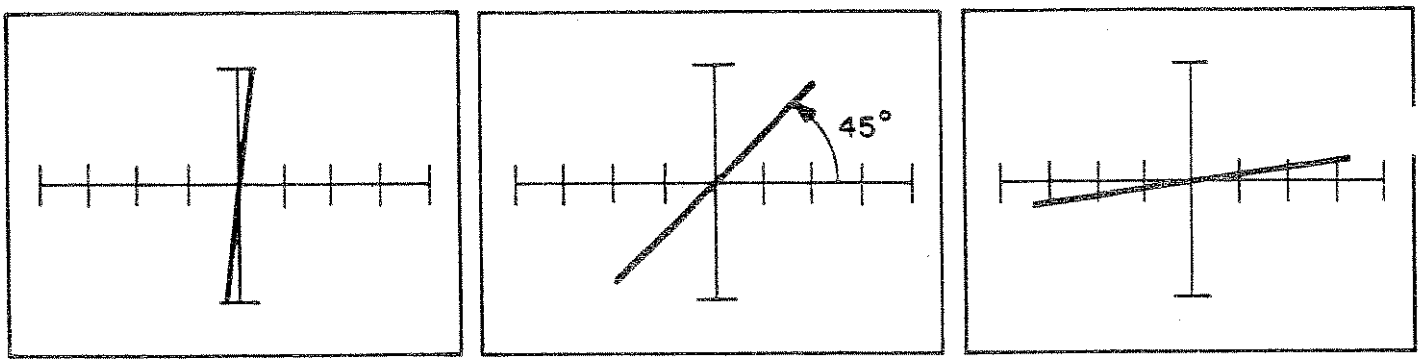


1 ohm Resistor | 50 ohm Resistor | 400 ohm Resistor

Figure 5-1. Effects of Resistance on the Rotation Angle — Low Range

5.1.2 Medium 1 Range

The medium 1 range is designed to detect resistance between 50 ohms and 10K ohms. Figure 5-2 shows the signatures for a 50 ohm resistor, a 1K resistor, and a 10K resistor using the medium 1 range. Resistors that are smaller than 50 ohms appear almost as a vertical line. A 1K resistor causes an angle of rotation of 45 degrees, while the display for a 10K resistor shows only slight rotation. Resistance values higher than 10K produce such a small rotation angle that it appears almost as a horizontal line.

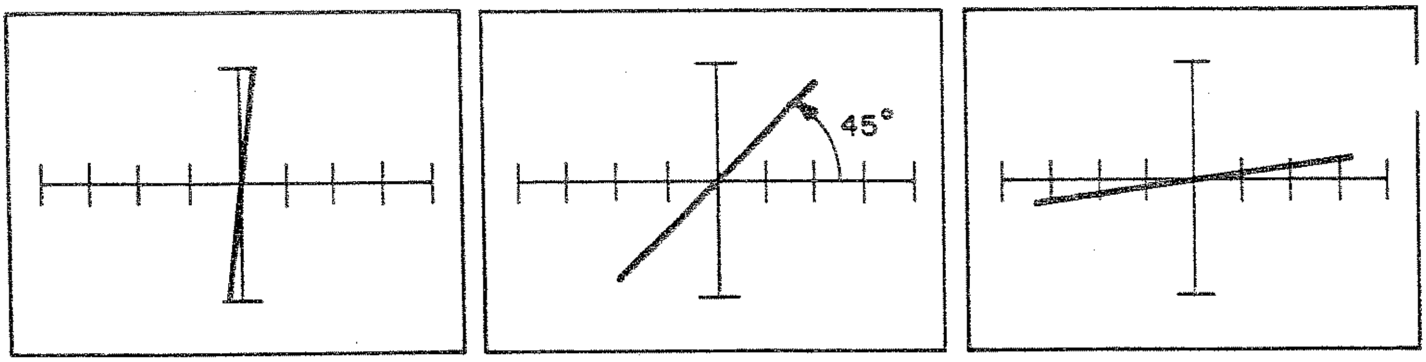


50 ohm Resistor | 1K Resistor | 10K Resistor

Figure 5-2. Effects of resistance on Rotation Angle — Medium 1 Range

5.1.3 Medium 2 Range

The medium 2 range is designed to detect resistance between 1K and 200K ohms. Figure 5-3 shows the signatures for a 1K resistor, a 15K resistor, and a 200K resistor using the medium 2 range. Resistance values smaller than 1K appear almost as a vertical line. A 15K resistor causes an angle of rotation of 45 degrees, while the display for a 200K resistor shows only slight rotation. Resistors higher than 200K produce such a small rotation angle that it appears almost as a horizontal line.

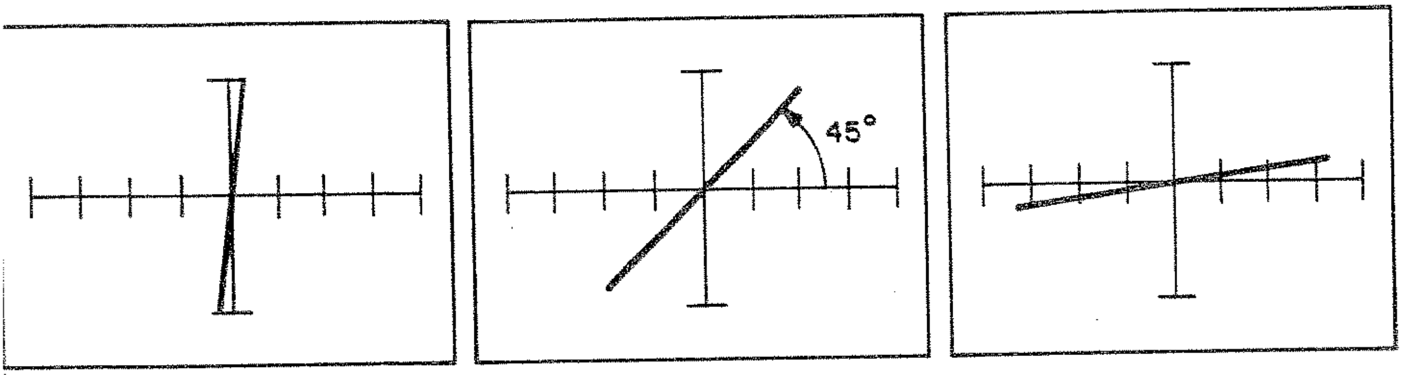


1K Resistor | 15K Resistor | 200K Resistor

Figure 5-3. Effects of Resistance on Rotation Angle — Medium 2 Range

5.1.4 High Range

The high range is designed to detect resistance between 3K and one Megohm. Figure 5-4 shows the signatures for a 3K resistor, a 50K resistor, and a one Megohm resistor using the high range. Resistors that are smaller than 3K appear almost as a vertical line. A 50K resistor causes an angle of rotation of 45 degrees, while the display for a one Megohm resistor shows only slight rotation. Resistance values higher than one Megohm produce such a small rotation angle that it appears almost as a horizontal line.



3K Resistor 50K Resistor 1M Resistor

Figure 5-4. Effects of Resistance on Rotation Angle — High Range

5.2 TESTING CAPACITORS

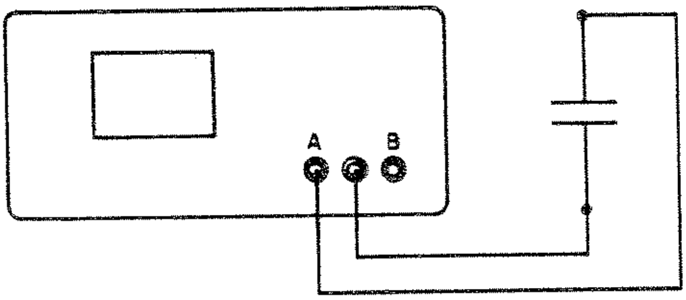


Figure 5-5. Capacitor Test Connections

With a capacitor connected to the Tracker 2000 as shown in Figure 5-5, the voltage, $V(t)$, across the capacitor is given as:

$$V(t) = a \, Sin \, (wt) \quad \ldots \quad (1)$$

The current in the loop, $I(t)$, is 90 degrees out of phase with respect to the voltage and is given as:

$$I(t) = b \, Cos \, (wt) \quad \ldots \quad (2)$$

where a and b are constants, and w is the test signal frequency.

From equation (1):

$$V(t)/a = Sin \, (wt)$$

or

$$V^2(t)/a^2 = Sin^2(wt) \quad \ldots \quad (3)$$

From equation (2):

$$I(t)/b = Cos \, (wt)$$

or

$$I^2(t)/b^2 = Cos^2 \, (wt) \quad \ldots \quad (4)$$

Adding equations (3) and (4):

$$V^2(t)/a^2 + I^2(t)/b^2 = Sin^2 \, (wt) + Cos^2 \, (wt) = 1 \quad \ldots \quad (5)$$

This is the equation of an ellipse. It becomes a circle if $a = b$. The size and shape of the ellipse depends on capacitor value, test signal frequency, and the selected impedance range.

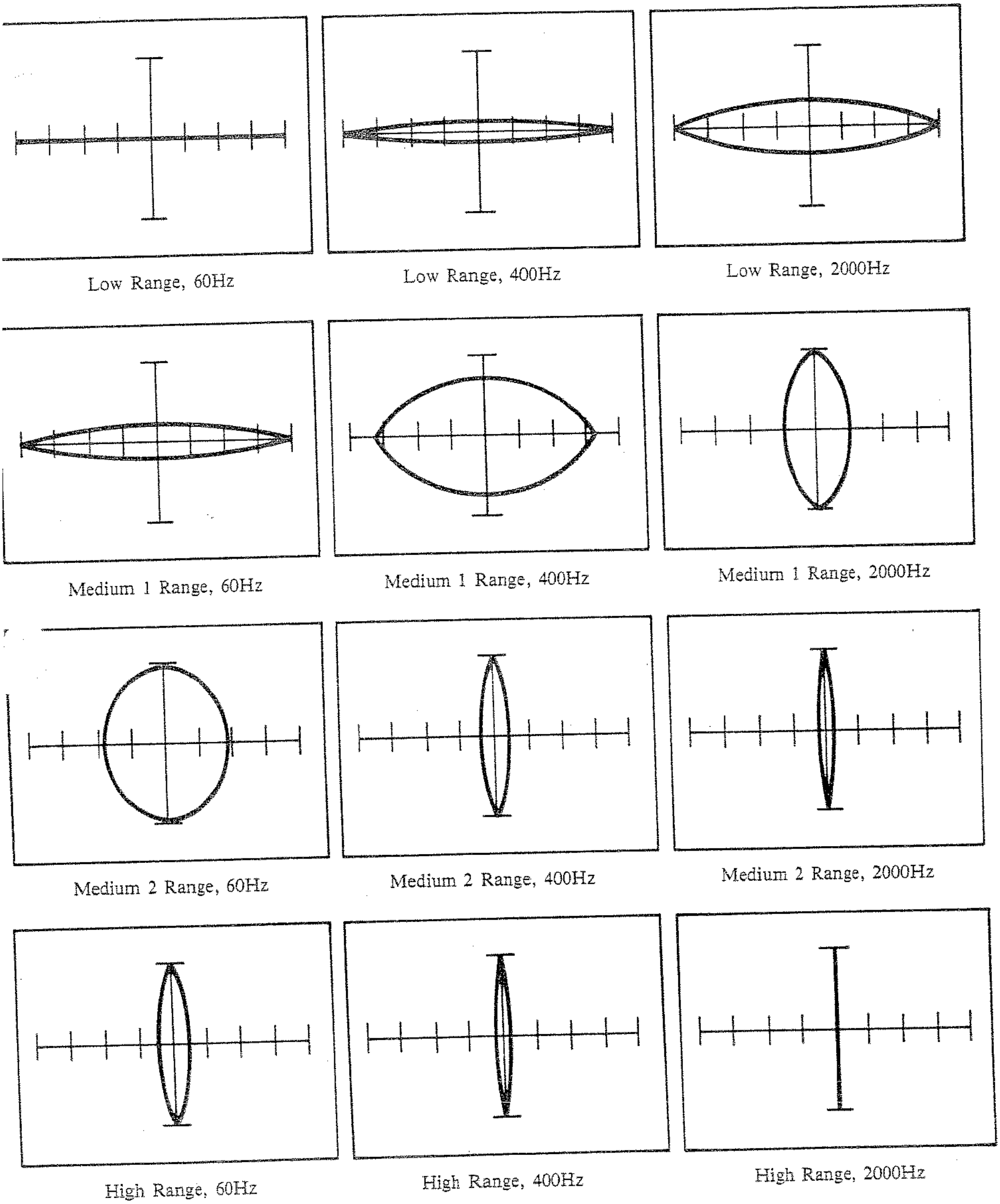


Figure 5-6. Signatures of a 0.22uF Capacitor

Figure 5-6 shows the signatures of a 0.22uF capacitor in each of the twelve combinations of range and frequency. Note that this value of capacitance appears to be an open circuit in the low range at 60Hz, while in the high range at 2000Hz this value is equivalent to a short circuit. In between the extremes this capacitor produces a variety of ellipsoids which demonstrates that certain range and frequency combinations are better than others for examining this particular value. Table 5-1 lists the range of capacitance covered by each of the twelve range and frequency combinations. The lowest value of capacitance in each combination gives a narrow horizontal ellipsoid on the display and capacitors less than the lower bound look like an open circuit. The upper bound of capacitance will produce a narrow vertical ellipsoid with capacitors of greater value appearing as the vertical line signature of a short circuit.

Table 5-1.

	50/60Hz			400Hz			2000Hz		
HIGH	.001uF	-	1uF	500pF	-	.1uF	100pF	-	.02uF
MED2	.01uF	-	2uF	.001uF	-	.5uF	200pF	-	.05uF
MED1	.02uF	-	50uF	.02uF	-	5uF	.005uF	-	1uF
LOW	5uF	-	2000uF	.5uF	-	100uF	.2uF	-	25uF

5.3 TESTING INDUCTORS

Inductors, like capacitors, produce elliptical signatures on the Tracker 2000 display. Figure 5-7 shows the test circuit for an inductor and Figure 5-8 shows the signatures produced in each of the twelve range and frequency combinations by a 250mH inductor.

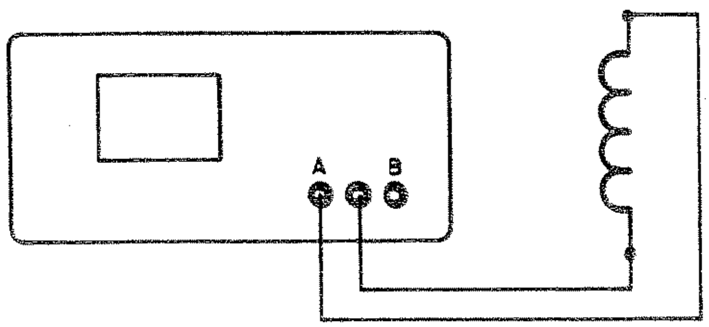
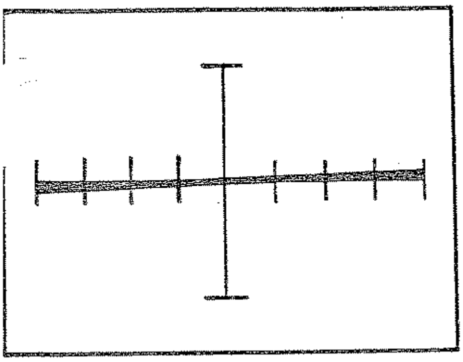
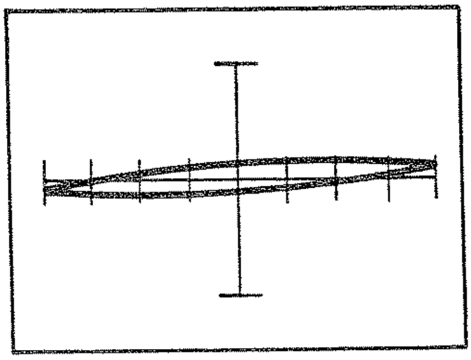


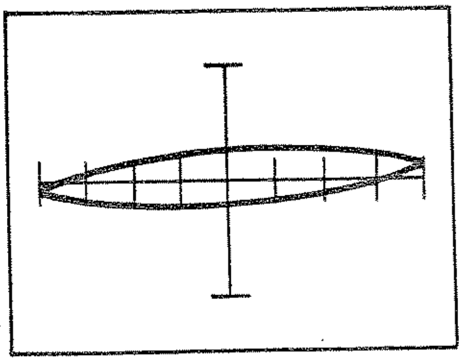
Figure 5-7. Inductor Test Connections



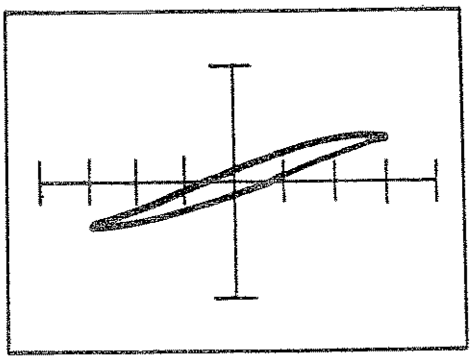
Low Range, 60Hz



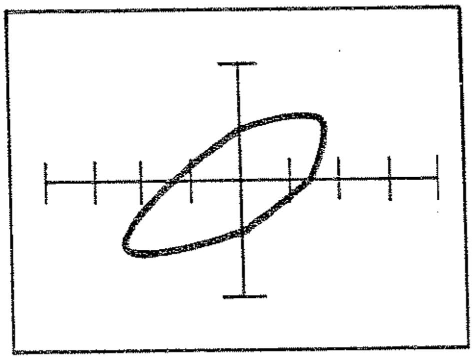
Low Range, 400Hz



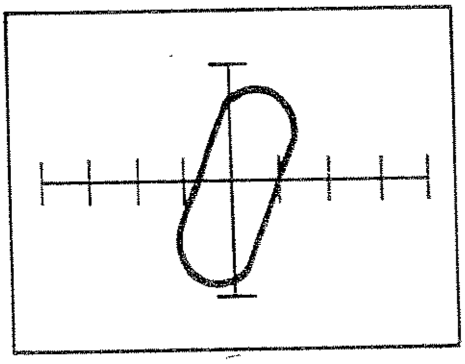
Low Range, 2000Hz



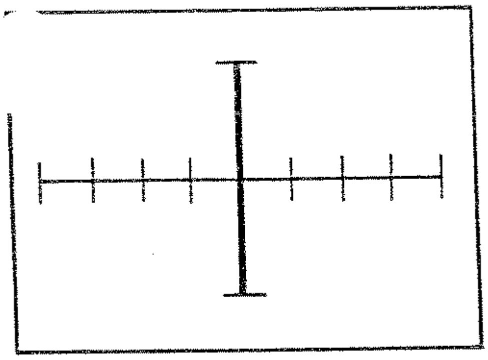
Medium 1 Range, 60Hz



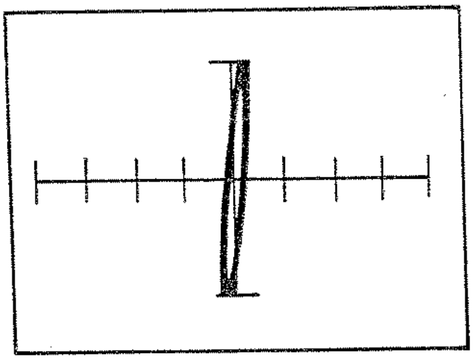
Medium 1 Range, 400Hz



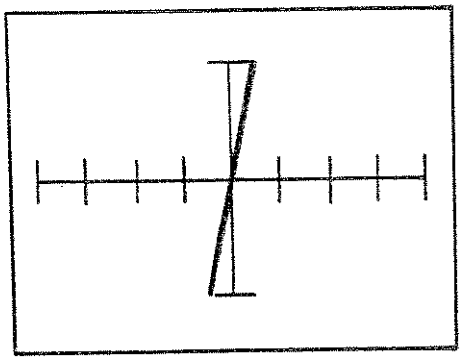
Medium 1 Range, 2000Hz



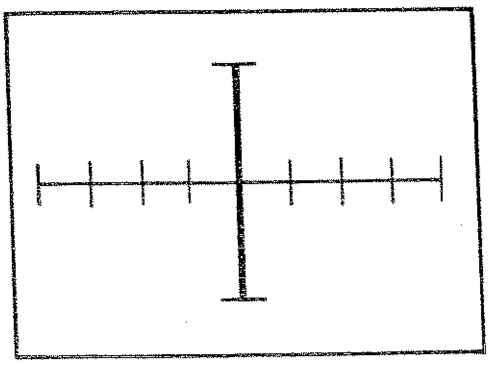
Medium 2 Range, 60Hz



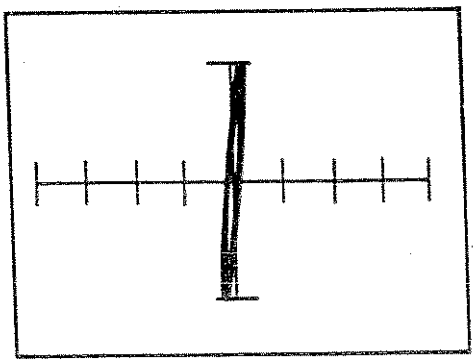
Medium 2 Range, 400Hz



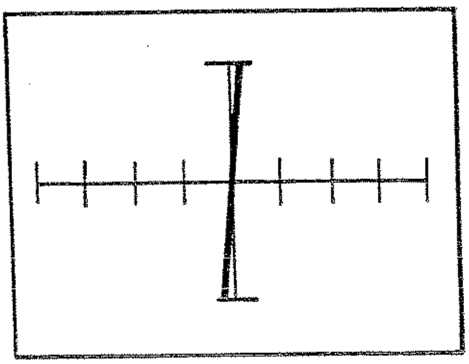
Medium 2 Range, 2000Hz



High Range, 60Hz



High Range, 400Hz



High Range, 2000Hz

Figure 5-8. Signatures of a 250mH Inductor

5.4 TESTING FERRITE INDUCTORS

Ferrite inductors can be checked with the Tracker 2000, but produce a signature that differs from the previously described inductor. Ferrite inductors operate well at high frequencies, but saturate at low frequencies. Figure 5-9 shows the signatures of a 490mH ferrite inductor tested at 60Hz. In low and medium 1 range the signatures show distortion. However, in medium 2 and high range, the impedance of the inductor is low compared with the internal impedance of the Tracker 2000 so the signatures are a "split" vertical trace.

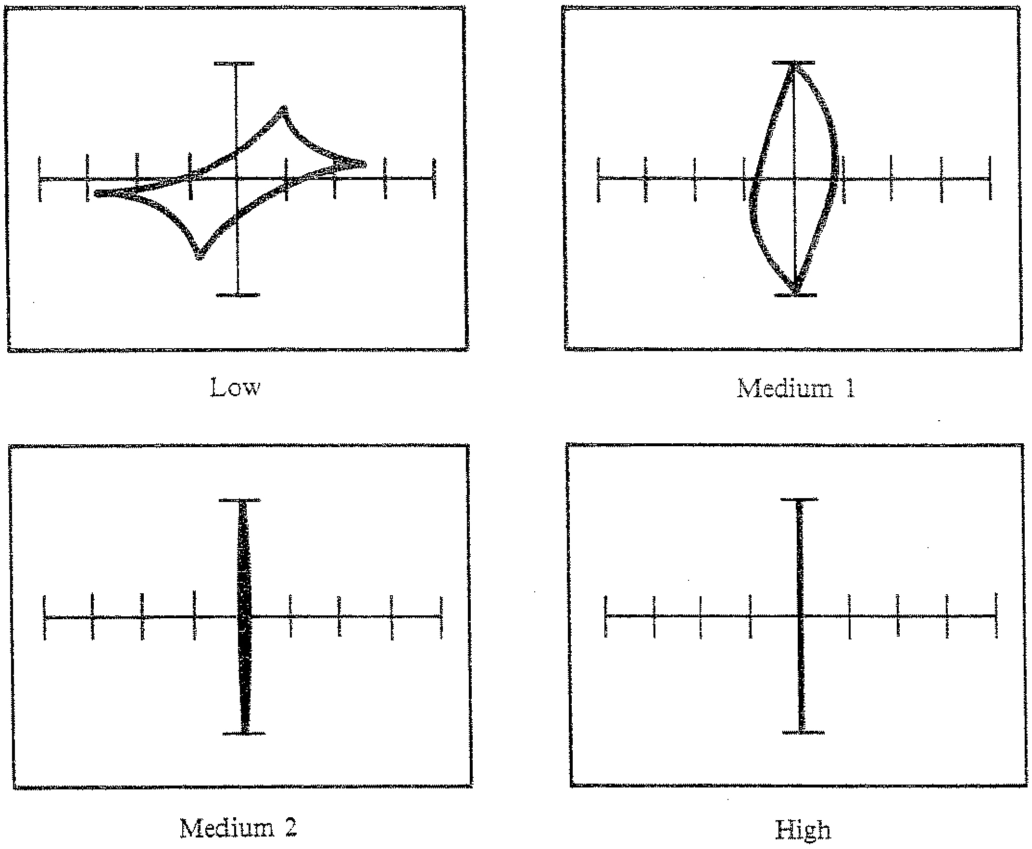


Figure 5-9. Signatures of 490mH Ferrite Inductor Tested at 60Hz

Figures 5-10 and 5-11 show the signatures of ferrite inductor at 400Hz and 2KHz respectively.

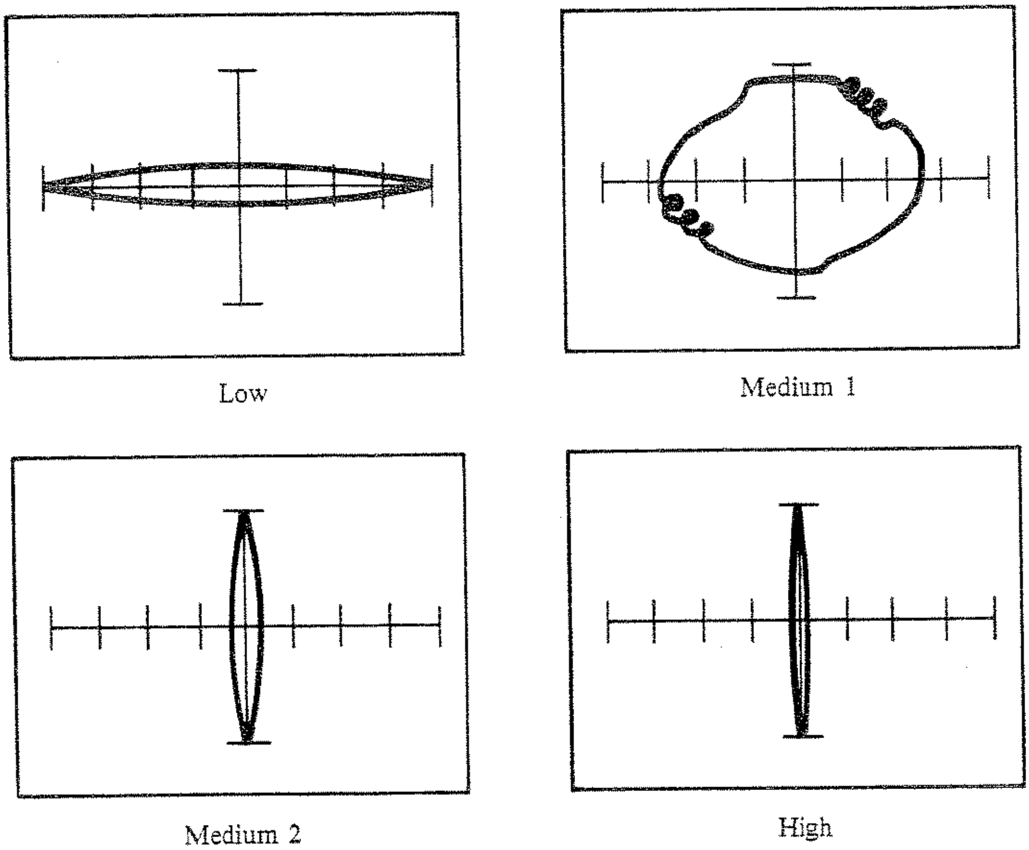


Figure 5-10. Signatures of 490mH Ferrite Inductor at 400Hz

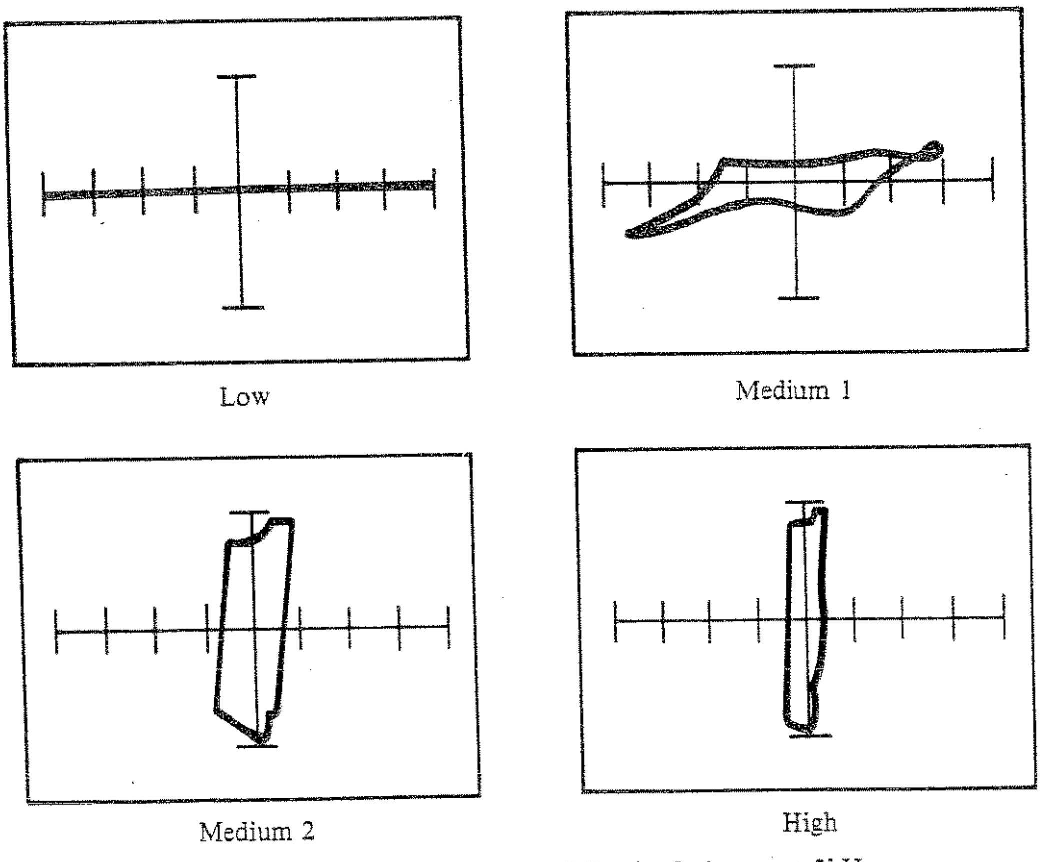


Figure 5-11. Signatures of 490mH Ferrite Inductor at 2kHz

Figure 6-3 shows the signatures for various resistors in parallel with the diode and medium 1 range selected on the Tracker 2000. Resistors with values greater than 50K have insignificant influence on the diode signature. For resistors of less than 500 ohms, the signature is dominated by the resistor, while the diode contributes little. The medium 2 and high range of the Tracker 2000 provide signatures similar to that of the medium 1 range, except that they cover higher resistance values.

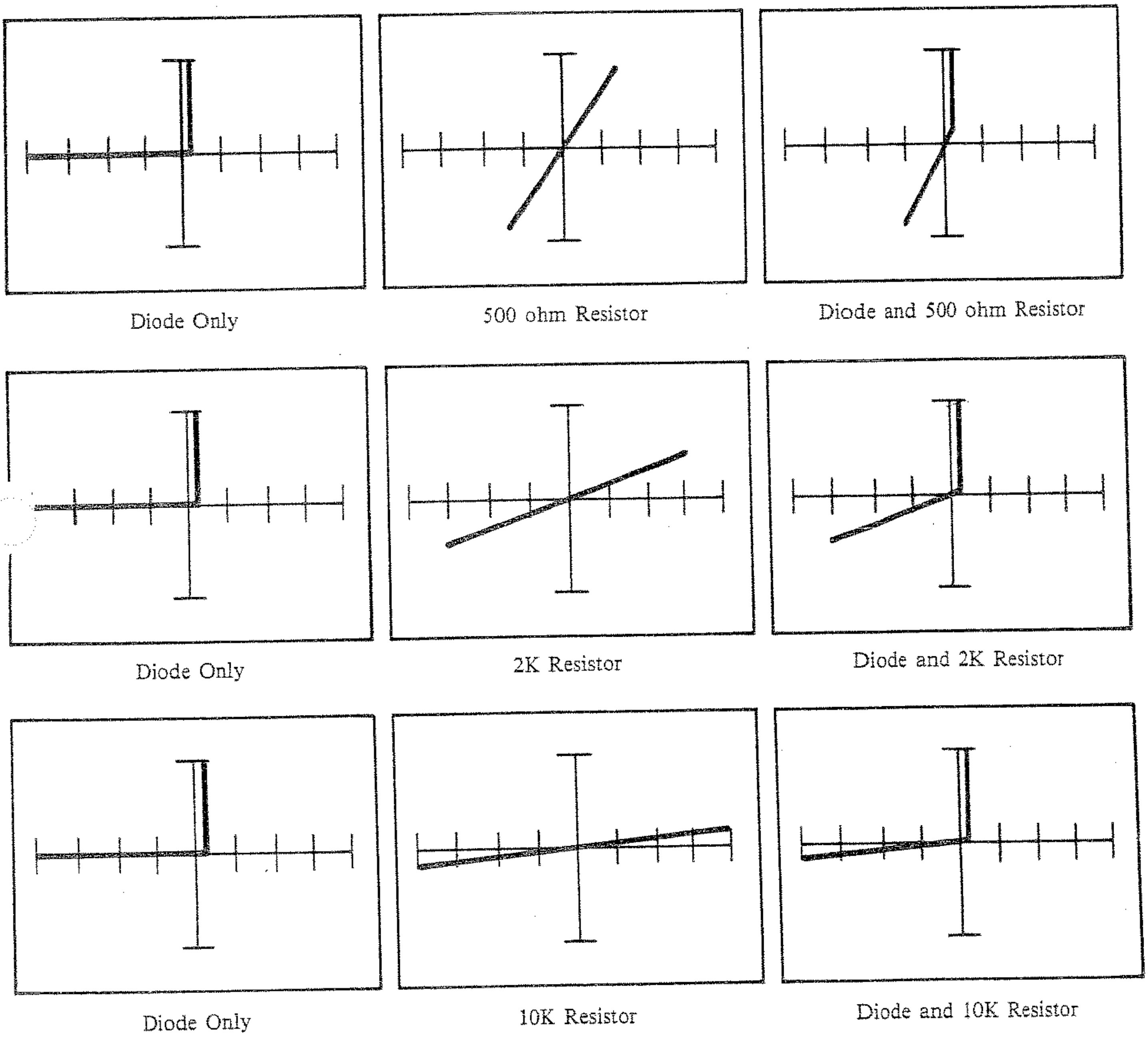


Figure 6-3. Parallel Diode/Resistor Signatures — Medium 1 Range

6.2.2 Diode In Series With a Resistor

Figure 6-4 shows the test circuit for a diode and resistor connected in series. When the diode is forward biased, it is in a low impedance state and the Tracker 2000 displays only the resistor. However, if the diode is reverse biased, the series circuit appears as an open circuit to the Tracker 2000. Figure 6-5 shows the equivalent circuits for the diode resistor series combination when forward and reverse biased.

Figures 6-6, 6-7, 6-8, and 6-9 show the Tracker 2000 signatures for various values of resistors in series with a diode while operating the Tracker 2000 in low, medium 1, medium 2, and high ranges.

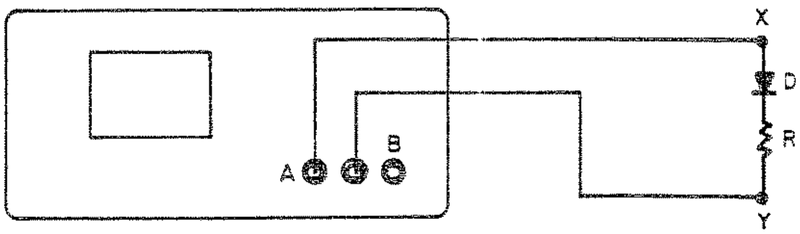


Figure 6-4. Test Circuit for a Series Diode and Resistor

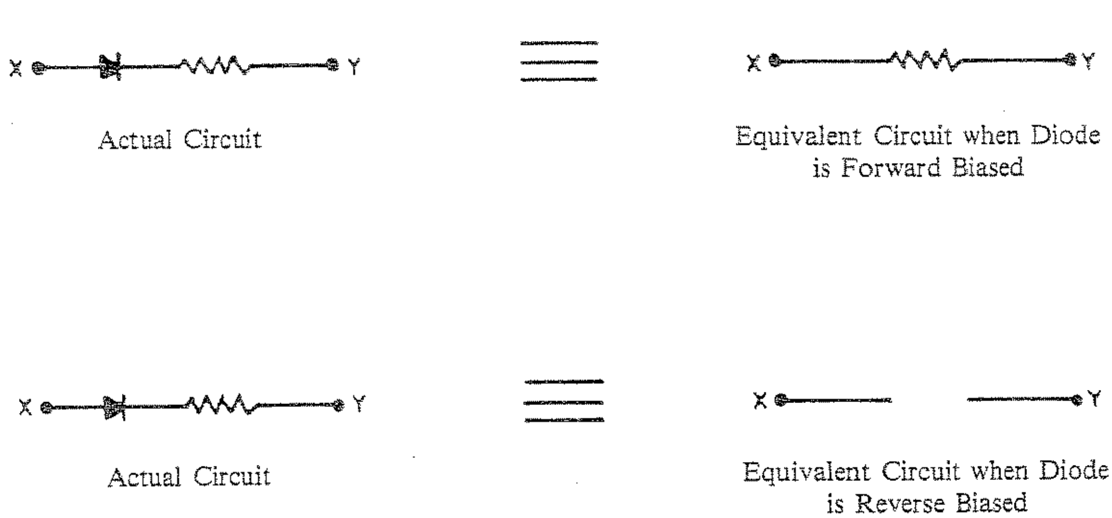
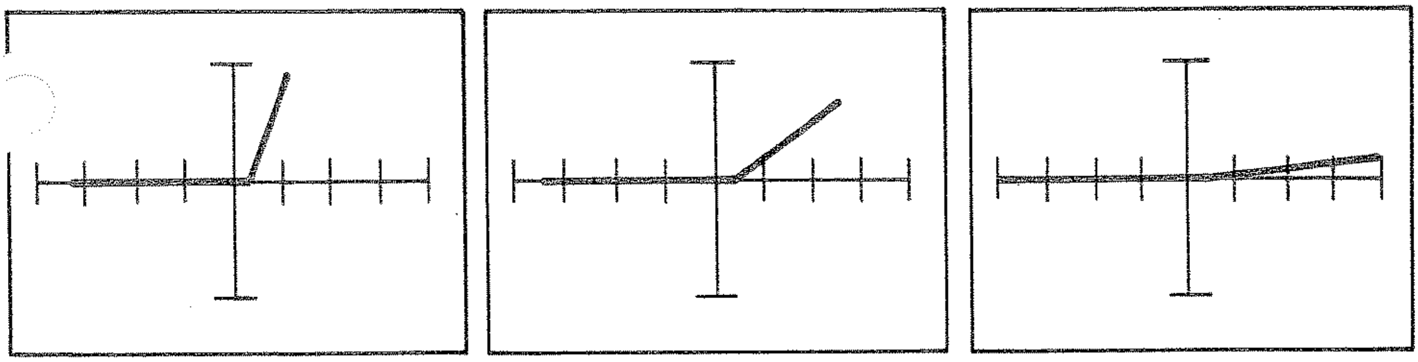
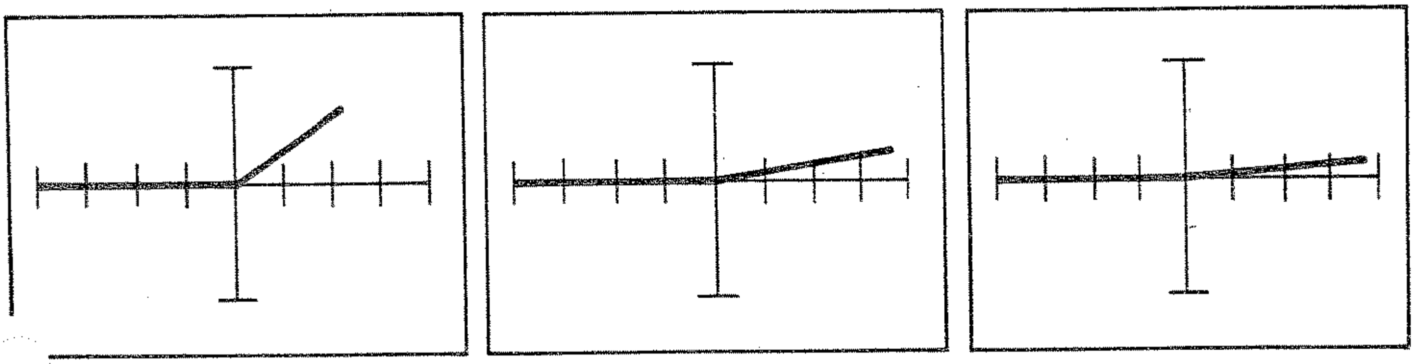


Figure 6-5. Diode/Resistor Equivalent Circuits



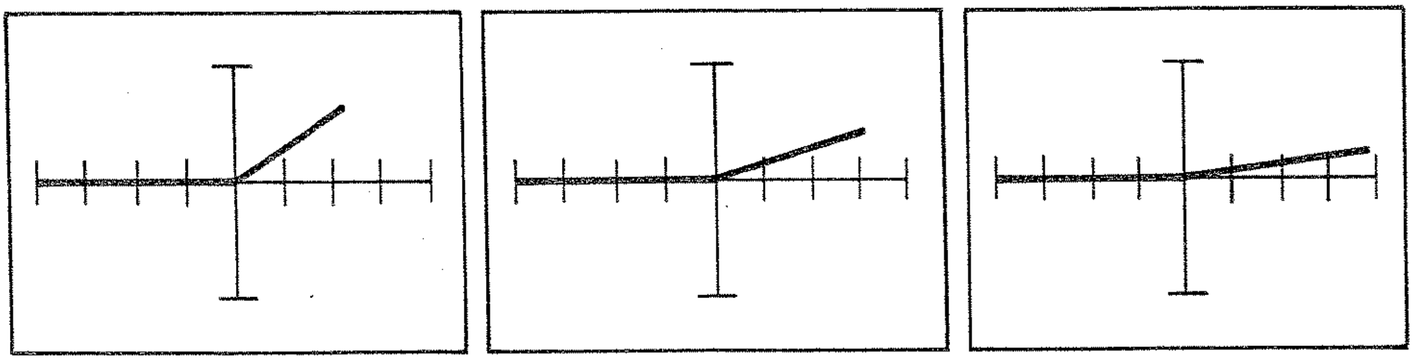
10 ohm Resistor | 50 ohm Resistor | 500 ohm Resistor

Figure 6-6. Low Range Signatures for Various Resistors and Series Diode at 60Hz



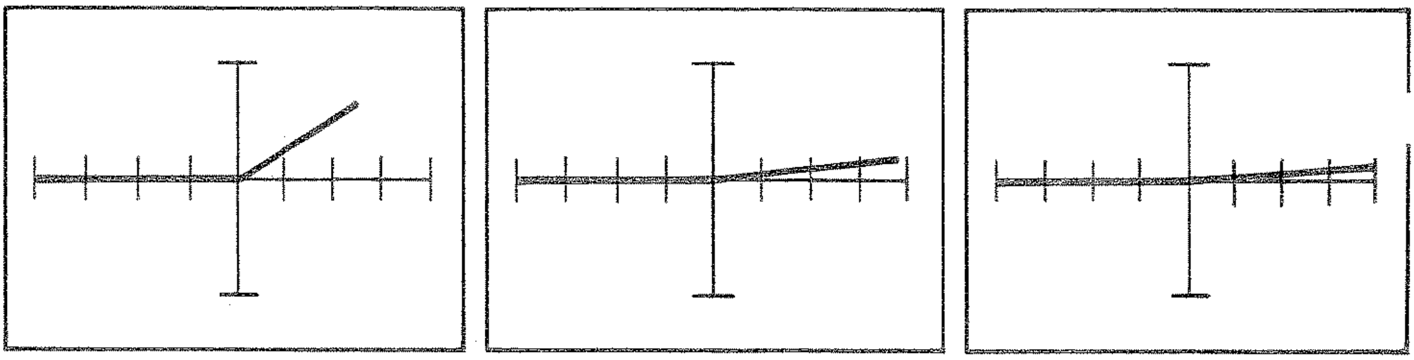
1K Resistor | 5K Resistor | 10K Resistor

Figure 6-7. Medium 1 Range Signatures for Various Resistors and Series Diode at 60Hz



20K Resistor | 50K Resistor | 100K Resistor

Figure 6-8. Medium 2 Range Signatures for Various Resistors and Series Diode at 60Hz



100K Resistor | 500K Resistor | 1M Resistor

Figure 6-9. High Range Signatures for Various Resistors and Series Diode at 60Hz

6.3 DIODE AND CAPACITOR PARALLEL COMBINATION

Figure 6-10 shows the test circuit for the parallel diode/capacitor combination.

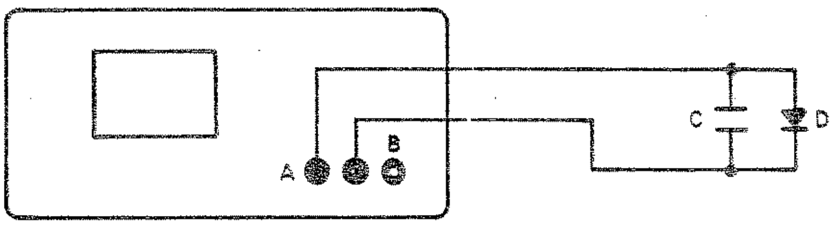
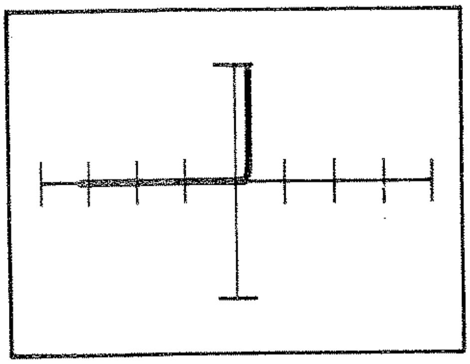


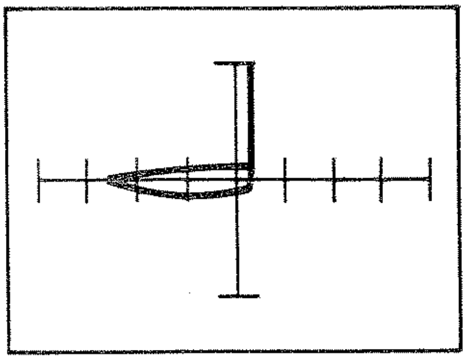
Figure 6-10. Test Circuit for Parallel Diode/Capacitor Combination.

Figure 6-11 shows signatures for a .1uF capacitor in parallel with a 1N4001 diode tested at 60Hz and 2KHz. At 60Hz, the low range is not able to detect the .1uF capacitor. The 2KHz test frequency is able to detect the .1uF capacitor in the low range. However, the diode effect is not detected at 2KHz in the medium 2 and high ranges.

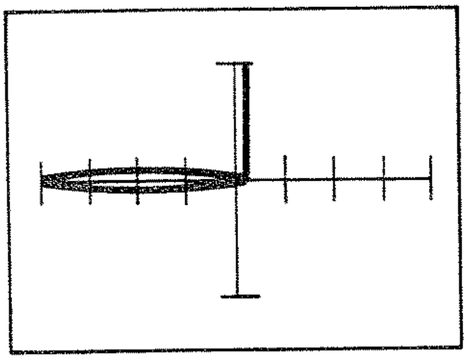
Figures 6-12 and 6-13 show the signatures of 1uF and 100uF capacitors respectively in parallel with a 1N4001 diode tested at 60Hz and 2KHz. For capacitors with a value larger than 100uF, the diode effect will no longer be detected in the medium 1, medium 2 and high ranges for all test frequencies.



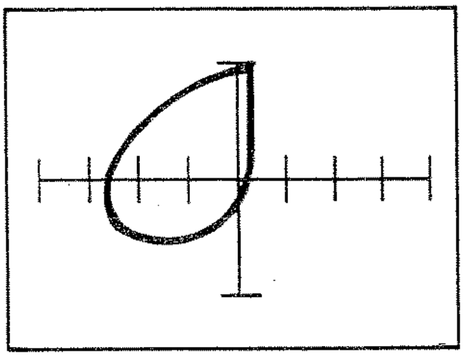
Low, .1uF, 60Hz



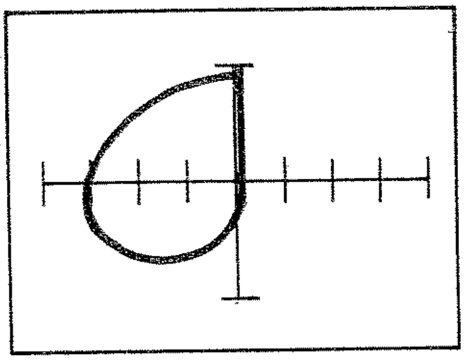
Low, .1uF, 2KHz



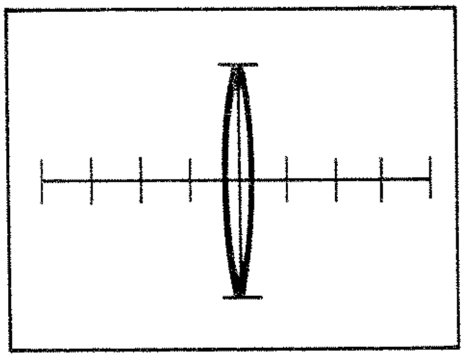
Medium 1, .1uF, 60Hz



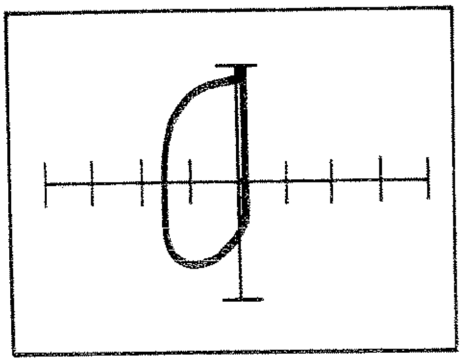
Medium 1, .1uF, 2KHz



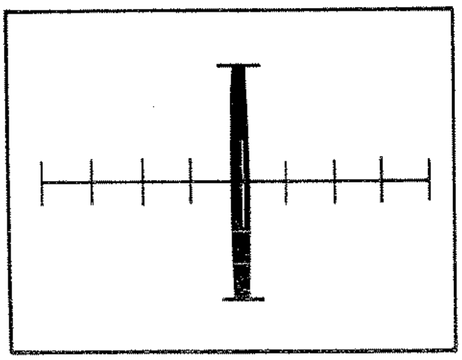
Medium 2, .1uF, 60Hz



Medium 2, .1uF, 2KHz

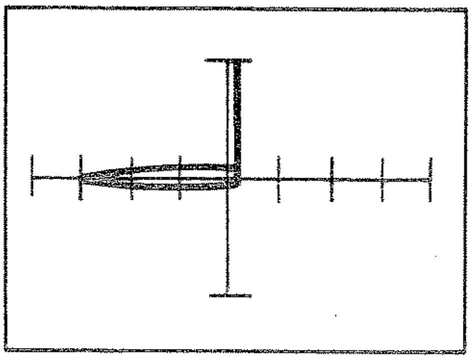


High, .1uF, 60Hz

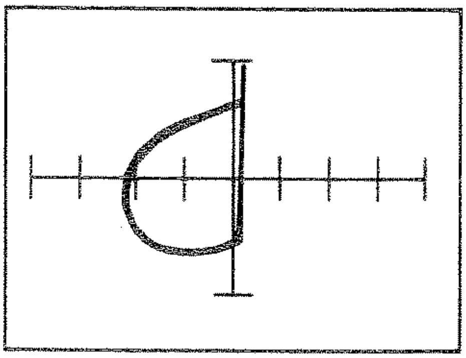


High, .1uF, 2KHz

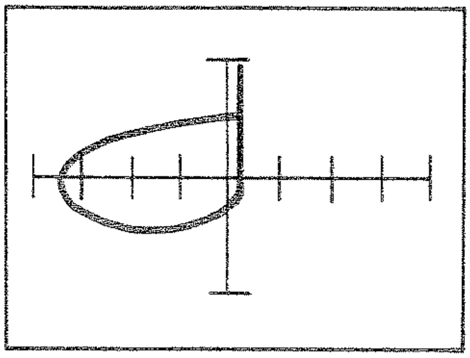
Figure 6-11. Signatures of .1uF Capacitor in Parallel with 1N4001 Diode Tested at 60Hz and 2KHz.



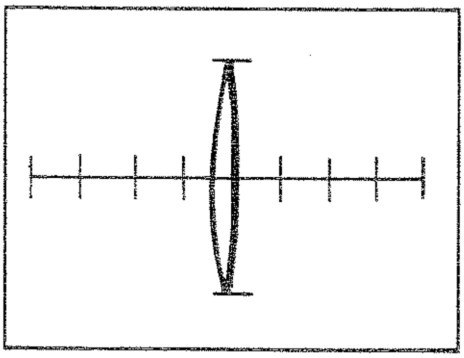
Low, 1uF, 60Hz



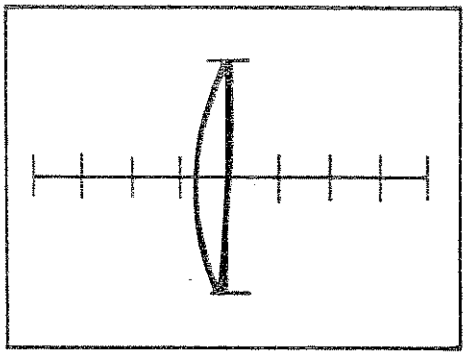
Low, 1uF, 2KHz



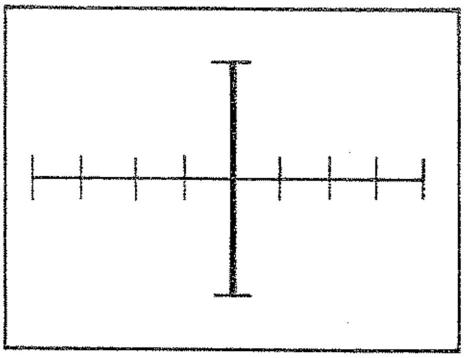
Medium 1, 1uF, 60Hz



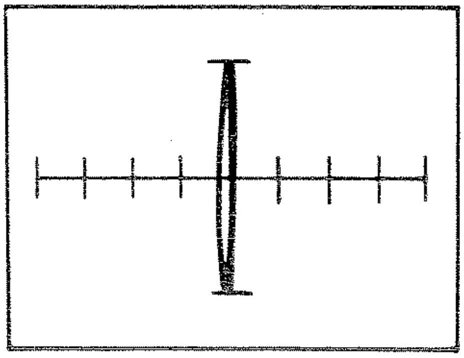
Medium 1, 1uF, 2KHz



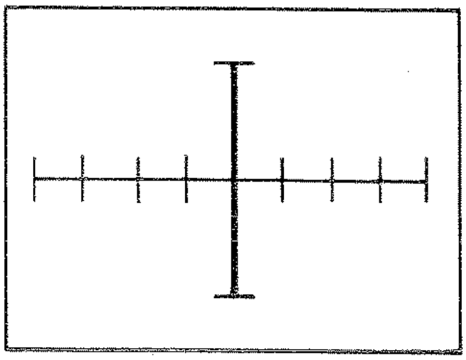
Medium 2, 1uF, 60Hz



Medium 2, 1uF, 2KHz

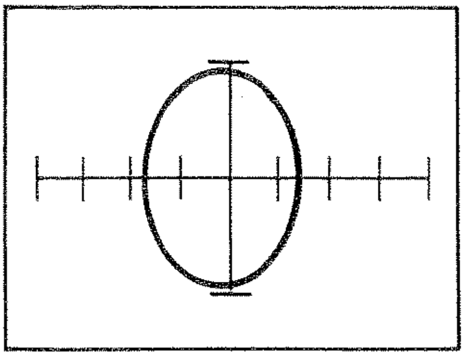


High, 1uF, 60Hz

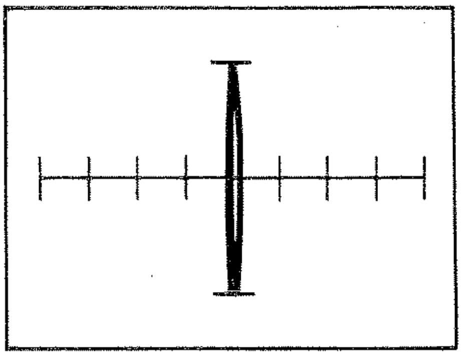


High, 1uF, 2KHz

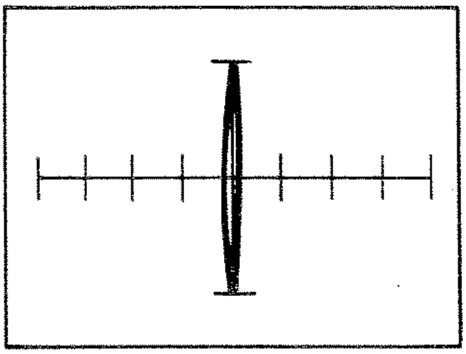
Figure 6-12. Signatures of 1uF Capacitor in Parallel with 1N4001 Diode Tested at 60Hz and 2KHz



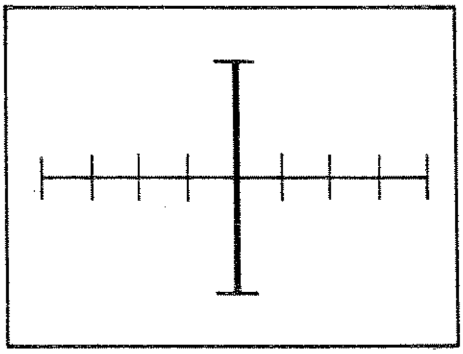
Low, 100uF, 60Hz



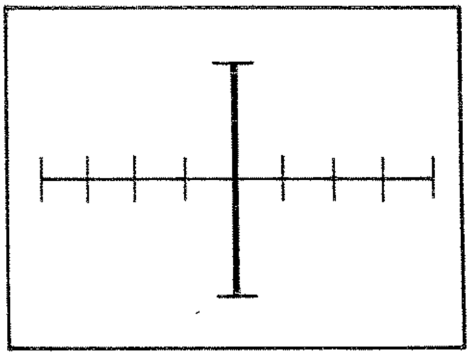
Low, 100uF, 2KHz



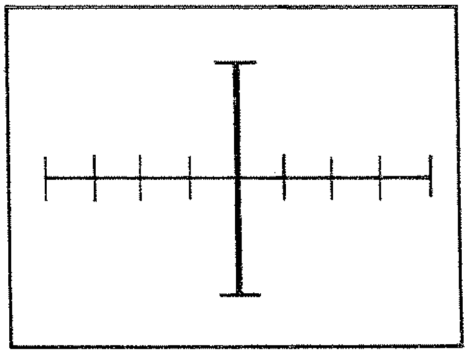
Medium 1, 100uF, 60Hz



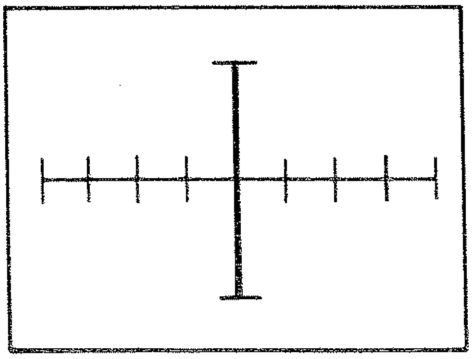
Medium 1, 100uF, 2KHz



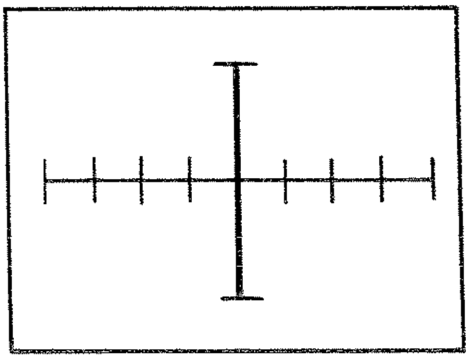
Medium 2, 100uF, 60Hz



Medium 2, 100uF, 2KHz



High, 100uF, 60Hz



High, 100uF, 2KHz

Figure 6-13. Signatures of 100uF Capacitor in Parallel with 1N4001 Diode Tested at 60Hz and 2KHz.

6.4 RESISTOR AND CAPACITOR PARALLEL COMBINATION

As previously discussed, a capacitor produces an ellipse, and a resistor produces trace rotation and amplitude reduction. Consequently, a resistor reduces the size of an ellipse and causes its major axis to rotate. The magnitude of the angle is determined by the value of the resistor and the range selected on the Tracker 2000. Figure 6-14 shows the test circuit for the parallel capacitor-resistor combination.

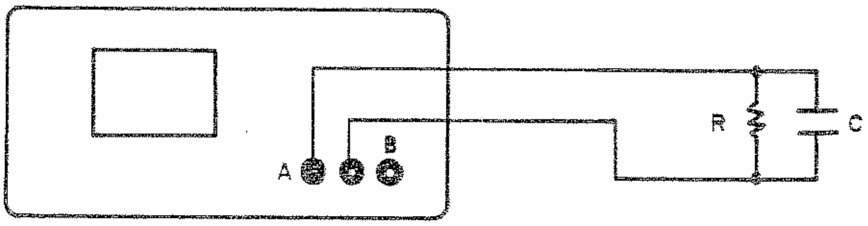
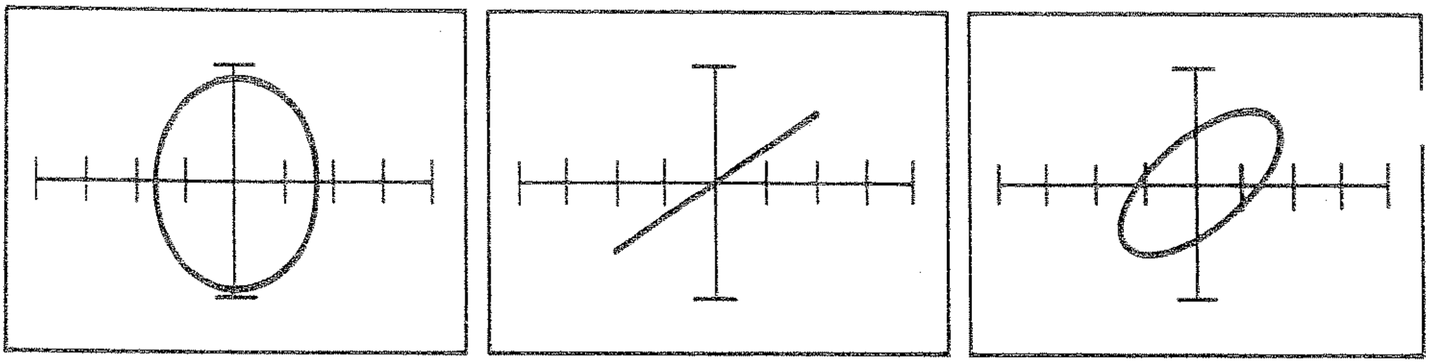


Figure 6-14. Test Circuit for Resistor and Capacitor in Parallel

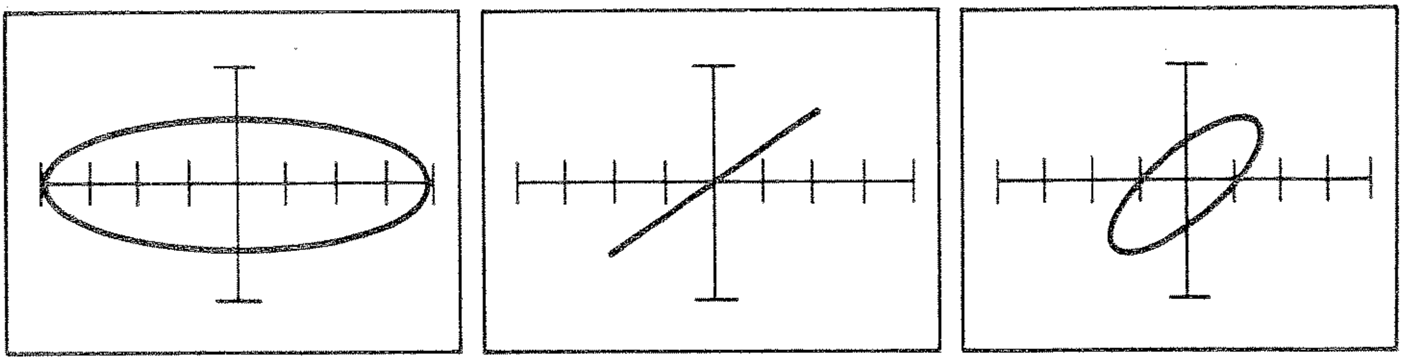
Figure 6-15 shows the effect of a 50K resistor on a .1uF capacitor (rotation and shrinkage of the ellipse).



.1uF Capacitor only | 50K Resistor only | Capacitor and Resistor in Parallel

Figure 6-15. Effects of a 50K ohm Resistor on a 0.1uF Capacitor in the High Range at 60Hz

Figure 6-16 shows the effect of a 1K resistor on 1uF capacitor.



1uF Capacitor only

1K Resistor only

Capacitor and Resistor in Parallel

Figure 6-16. Effect of a 1K Resistor on a 1uF Capacitor in the Medium 1 Range at 60Hz

6.5 INDUCTOR IN PARALLEL WITH A DIODE

This type of circuit is found in relays and line printers. The diode suppresses the high voltage "kick" produced when the inductor or coil is de-energized. To test this device combination, connect the Tracker 2000 probes as shown in Figure 6-17.

Figure 6-18 displays signatures of a 1N4001 diode in parallel with an Aromat relay HB1E-DC12.

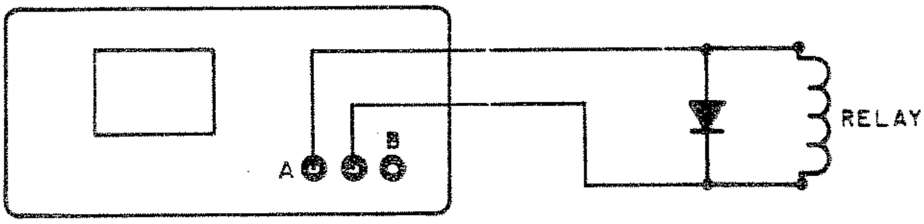


Figure 6-17. Inductance/Diode Combination

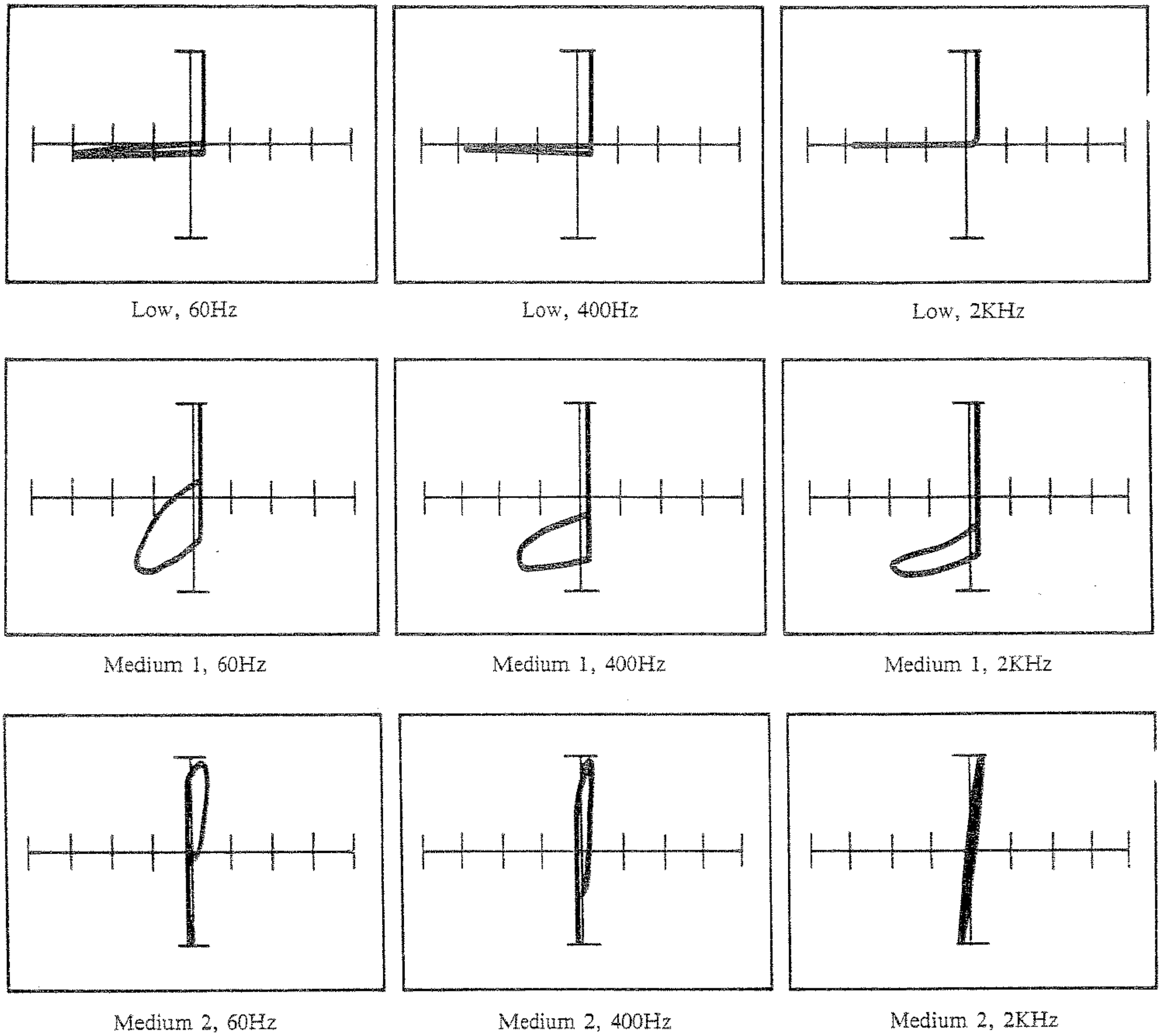


Figure 6-18. Signatures of a 1N4001 Diode in Parallel with an Aromat relay HB1E-DC12.

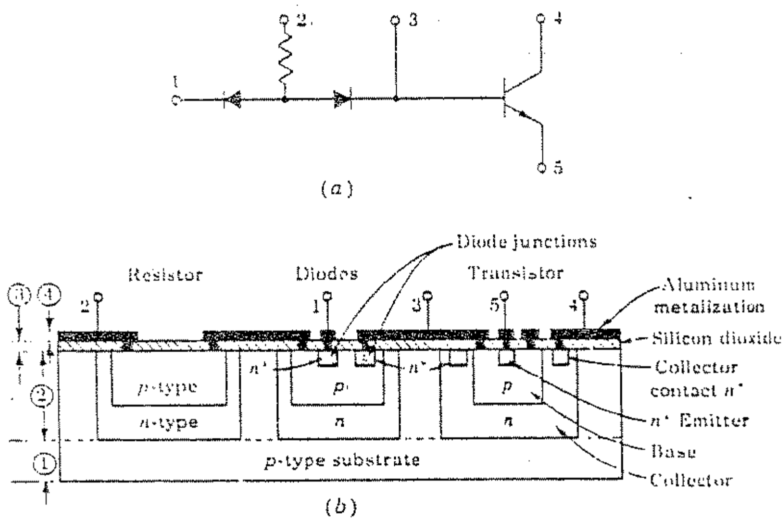
SECTION 7
TESTING INTEGRATED CIRCUITS

7.1 INTRODUCTION

7.1.1 Integrated Circuit Technology

An integrated circuit consists of a single-crystal chip of silicon, typically 50 x 50 mils in cross-section, containing both active and passive elements, plus their interconnections. Such circuits are produced by the same processes used to fabricate individual transistors and diodes. These processes include epitaxial growth, masked impurity diffusion, oxide growth, and oxide etching, using photolithography for pattern definition.

The basic structure of an integrated circuit is shown in Figure 7-1, and consists of four distinct layers of material. The bottom layer (1) (6 mils thick) is P-type silicon and serves as a substrate upon which the integrated circuit is to be built. The second layer (2), typically 25 mils thick, is an N-type layer which is grown as a single-crystal extension of the substrate. All components are built within the N-type layer using a series of diffusion steps. The third layer of material (3) is silicon dioxide, and it also provides protection of the semiconductor surface against contamination. Finally, a fourth metallic (aluminum) layer (4) is added to supply the necessary interconnections between components.



(a) A circuit containing a resistor, two diodes, and a transistor. (b) Cross-sectional view of the circuit in (a) when transformed into a monolithic form (not drawn to scale). The four layers are (1) substrate, (2) n-type crystal containing the integrated circuit, (3) silicon dioxide, and (4) aluminum metalization.
to scale.)

Figure 7-1. Typical Integrated Circuit Construction

7.1.2 Integrated Circuit Testing Techniques

This manual has discussed the techniques of testing resistors, capacitors, inductors, diodes, and transistors. All these techniques can be applied to test integrated circuits. The Tracker 2000 signatures produced across any two pins of an integrated circuit is the resultant effect of resistors, diodes, transistors, and capacitors. Apply the Tracker 2000 probes between two pins on an integrated circuit to display the resultant signature of these composite components.

This section provides information related to testing the following devices:

- Linear operational amplifiers
- Linear voltage regulators
- 555 timers
- TTL digital ICs
- Low power Schottky digital ICs
- CMOS digital ICs
- MOS static RAMs
- EPROMs
- Bipolar PROMs
- Digital-to-Analog converters
- Microprocessors

To test an integrated circuit, the Tracker 2000 leads are connected to two pins at a time. Since the typical integrated circuit has many pins, the number of possible testing combinations becomes very large; for example, a 16 pin device has 120 possible two pin combinations. It becomes impractical to test all possibilities, and our experience has shown that it is adequate to test the input and output pins with respect to V+ and V− in order to determine whether a device is good or bad.

7.2 LINEAR OPERATIONAL AMPLIFIERS

When checking an analog device or circuit, the low range is used most of the time. Analog circuits have many more single junctions to examine. Analog flaws are easier to detect in the low range. The 55 ohm internal impedance of the low range makes it less likely that other components, in parallel with the device under test, will load the Tracker 2000 sufficiently to modify the signatures produced if the device were tested out of circuit.

When checking an op amp in-circuit, it is almost mandatory to do a direct comparison with a known good circuit because the many different feedback loops associated with op amps may cause an almost infinite number of signatures. Figure 7-2 shows the schematic and connection diagram of a National Semiconductor 1458 Op Amp.

Figures 7-3 through 7-6 show the signatures between pin 8 (V+) and the other pins of the LM1458, while Figures 7-7 through 7-9 show the signatures between pin 4 (V−) and the other pins.

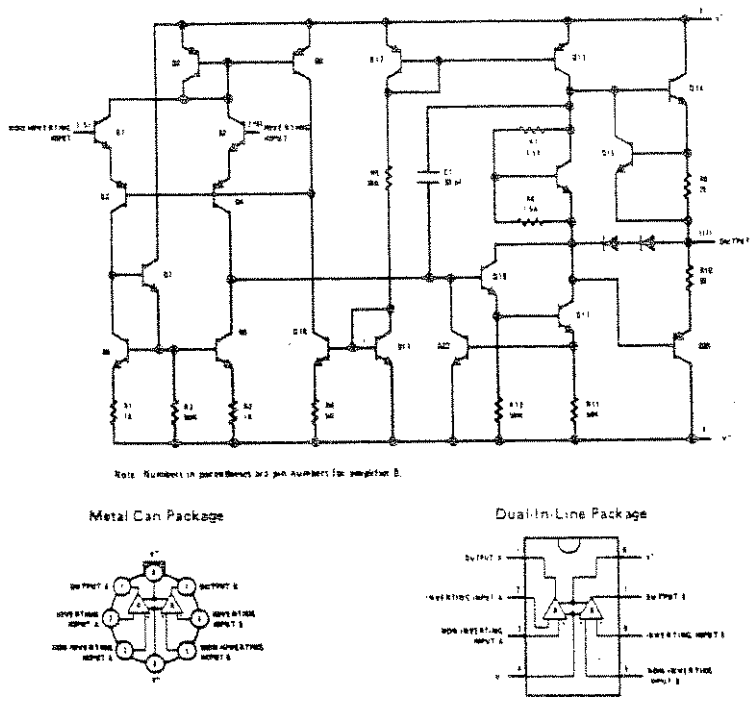


Figure 7-2. The LM1458 Op-Amp, Schematic and Connections

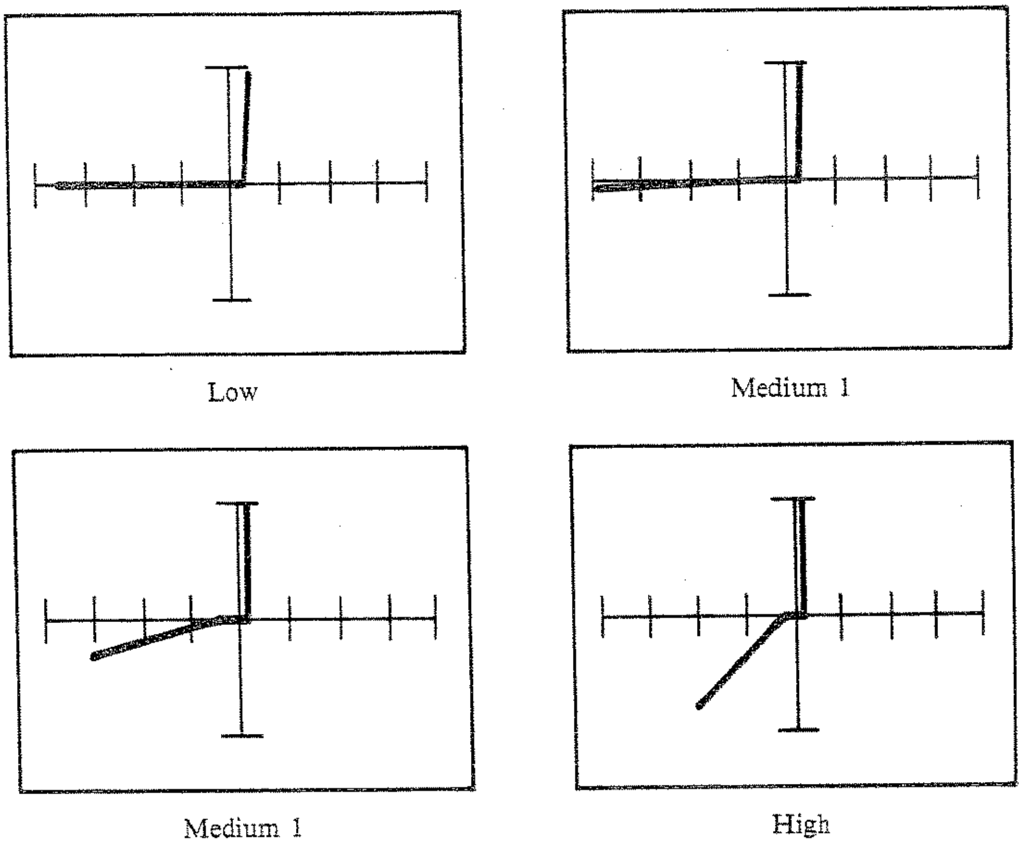


Figure 7-3. Signatures Between Pin 4 (V−) and Pin 8 (V+) of an LM1458 at 60Hz

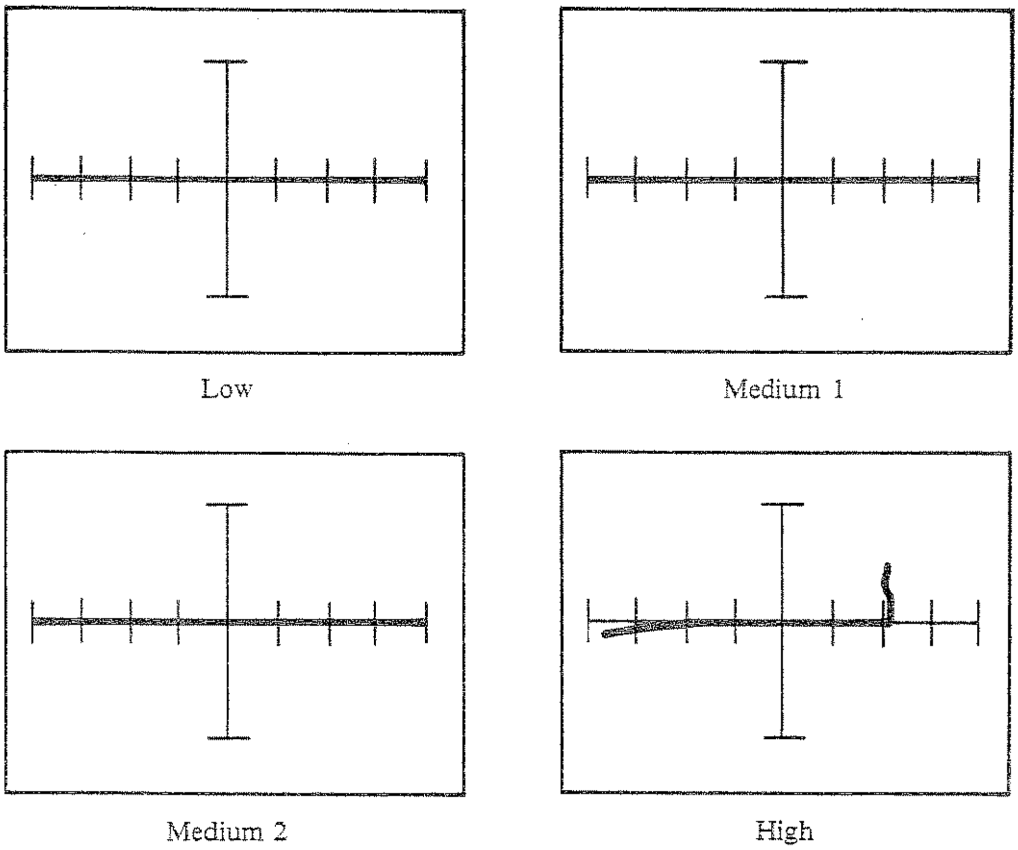


Figure 7-4. Signatures Between Pin 2 (Inverting Input) and Pin 8 (V+) of an LM1458 at 60Hz

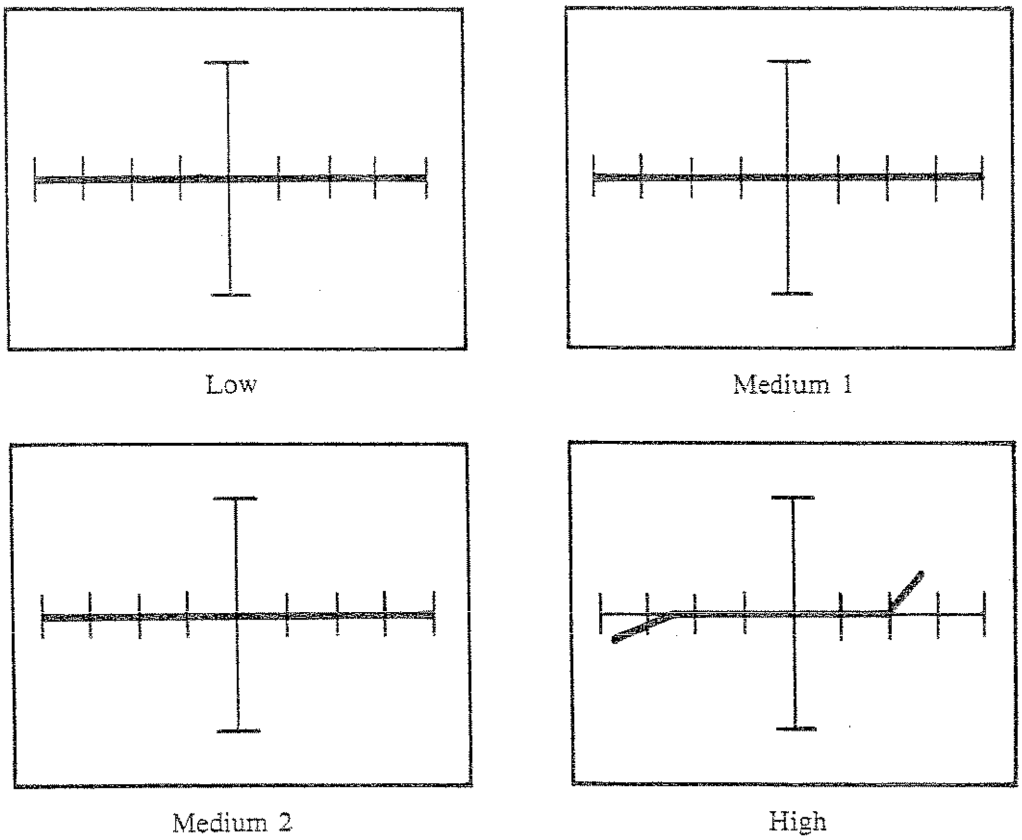


Figure 7-5. Signatures Between Pin 3 (Non-Inverting Input) and Pin 8 (V+) of an LM1458 at 60Hz

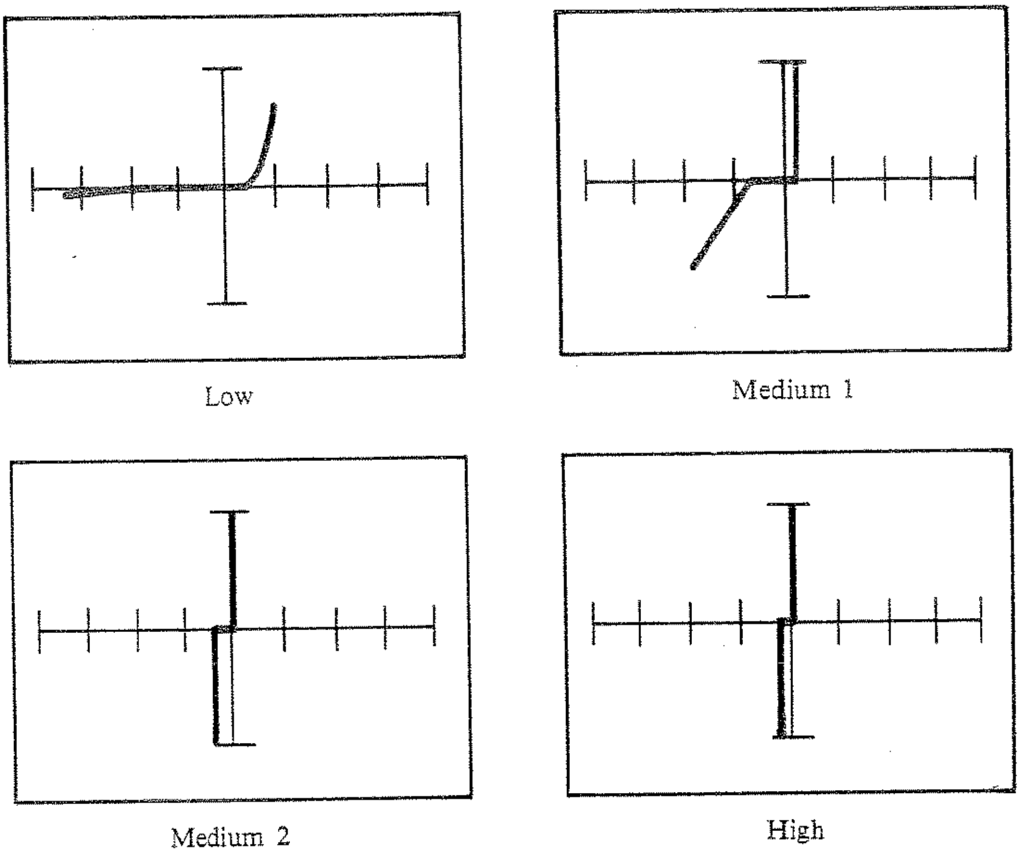


Figure 7-6. Signatures Between Pin 1 (Output) and Pin 8 (V+) of an LM1458 at 60Hz

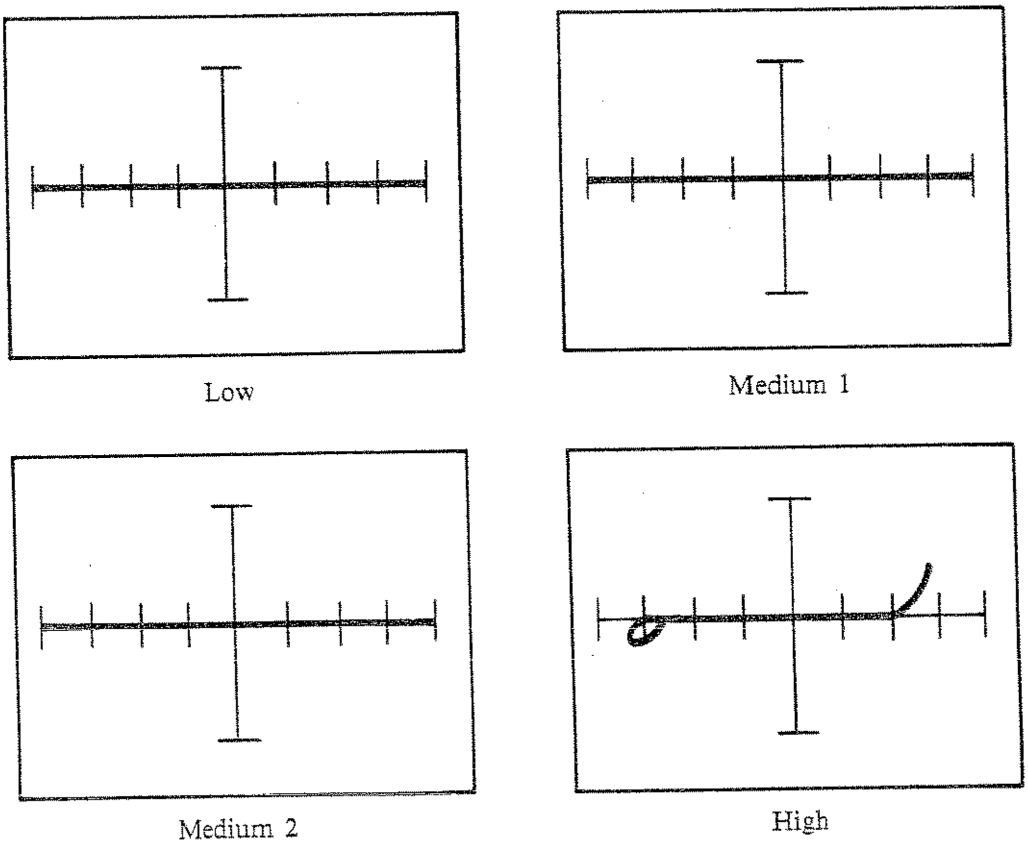


Figure 7-7. Signatures Between Pin 2 (Inverting Input) and Pin 4 (V−) of an LM1458 at 60Hz

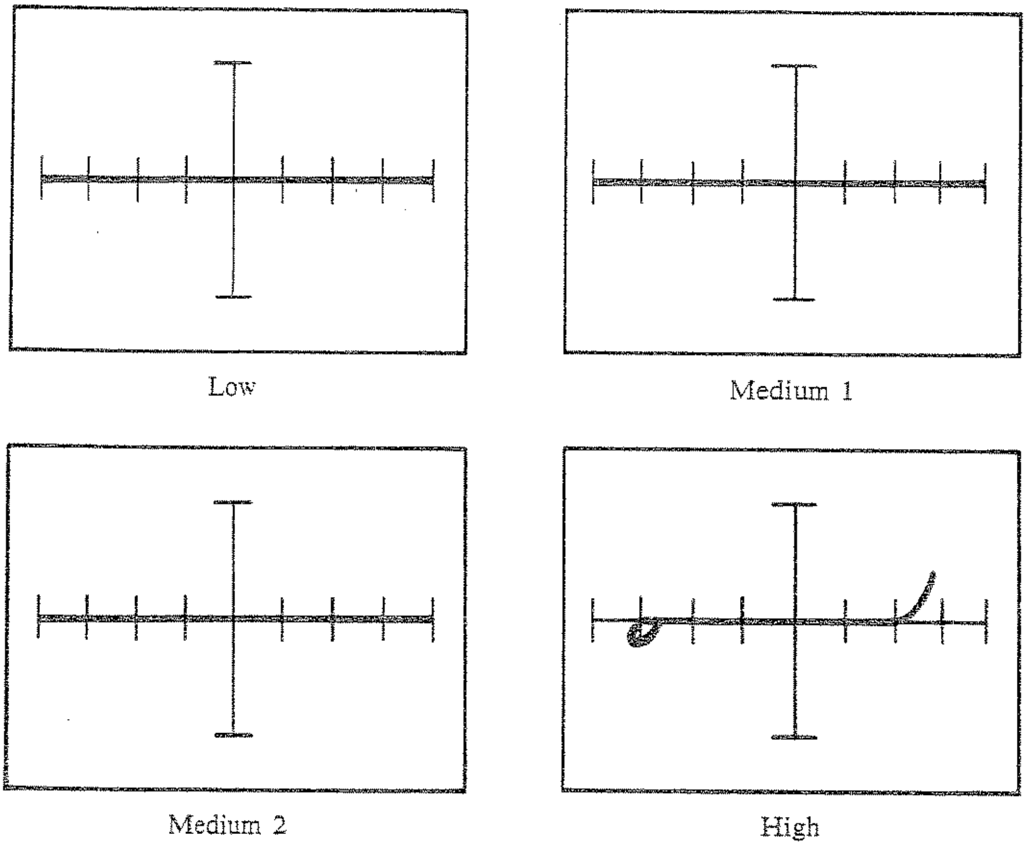


Figure 7-8. Signatures Between Pin 3 (Non-Inverting Input) and Pin 4 (V−) of an LM1458 at 60Hz

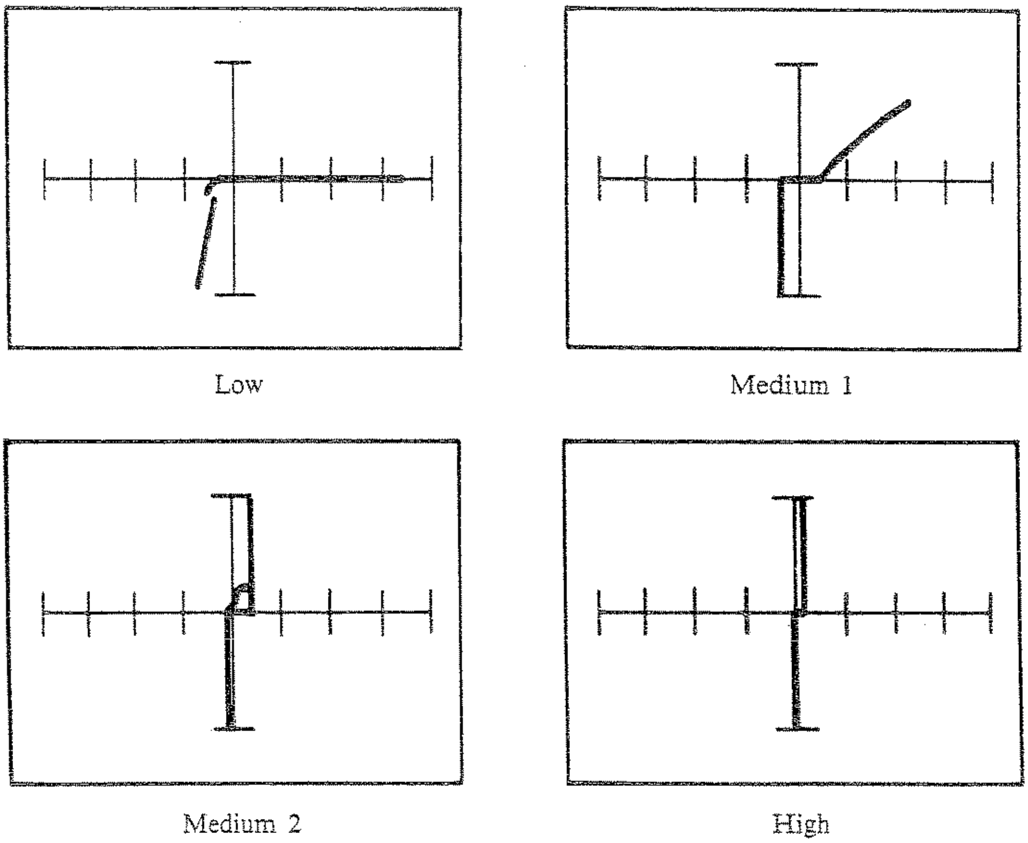


Figure 7-9. Signatures Between Pin 1 (Output) and Pin 4 (V−) of an LM1458 at 60Hz

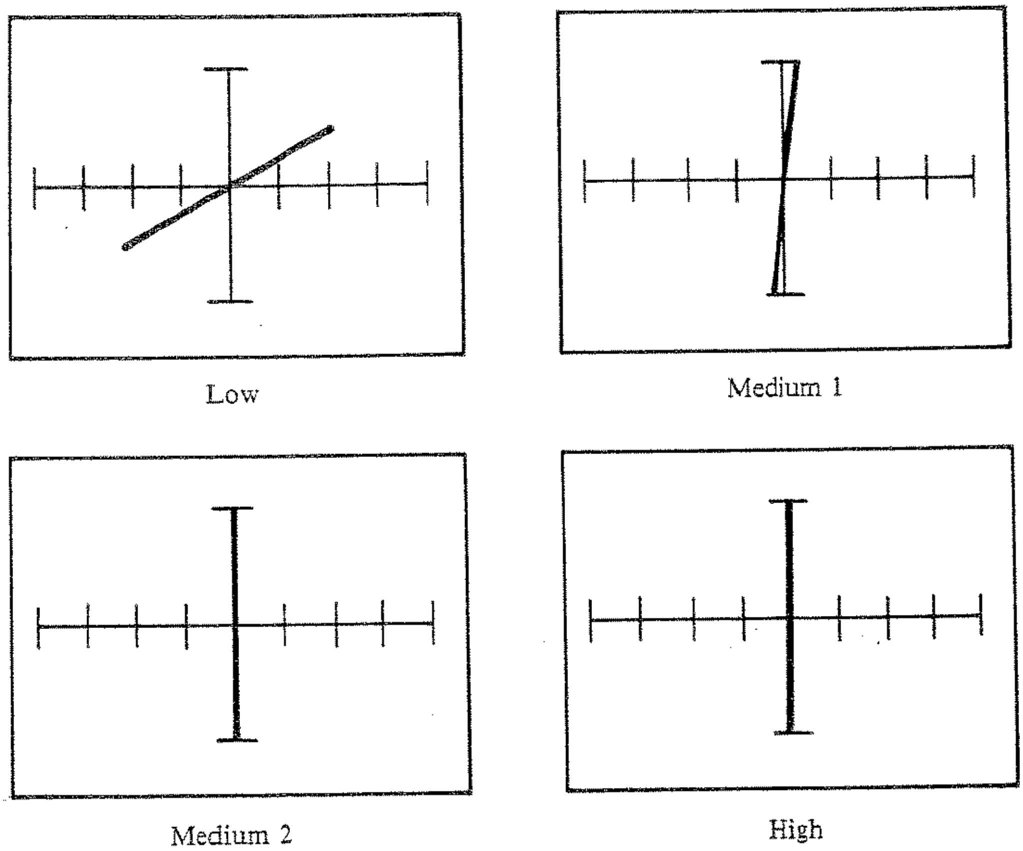


Figure 7-10. Signatures Between Pin 4 (V−) and Pin 8 (V+) of a Defective LM1458 at 60Hz

7.3 LINEAR VOLTAGE REGULATORS

Voltage regulators, especially the 7800 and 7900 series, are used in many pieces of electronic equipment.

7.3.1 The 7805 Regulator

Figure 7-11 shows the schematic and the connection of a 7805 +5V regulator. Figure 7-12 shows the test connections to the 7805 voltage regulator terminals. Figures 7-13 through 7-15 show the test signatures for a 7805. Different manufacturers implement their products with different topologies and it is expected that the signatures will vary for the same devices from different manufacturers. Figure 7-16 shows the signatures of a defective 7805. There is a substantial difference in the signature between a good and defective device in the low and medium 1 ranges.

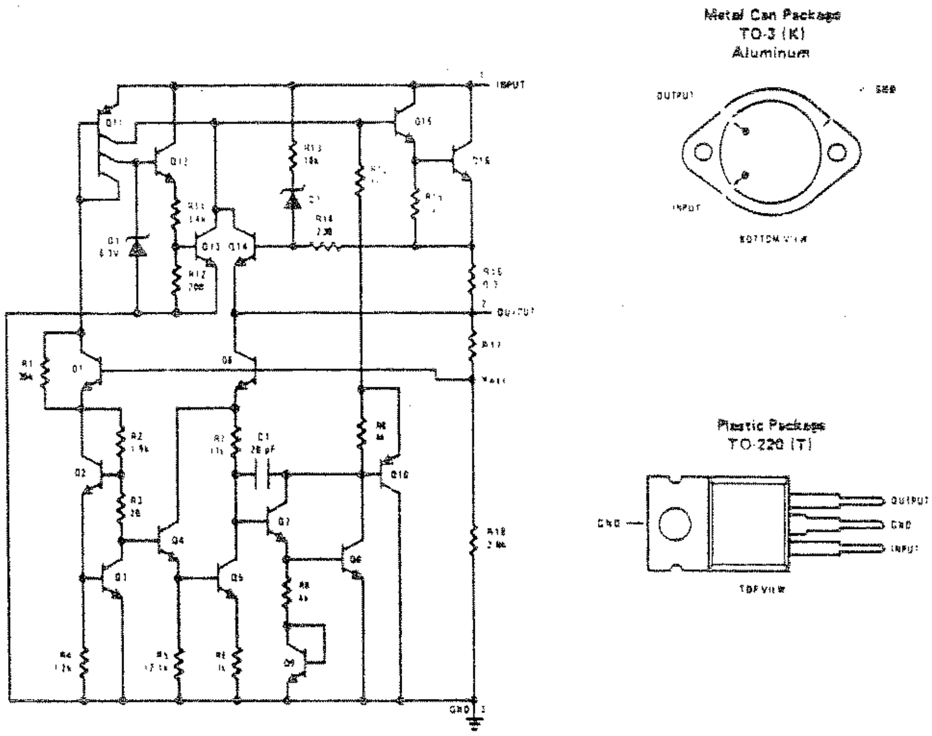


Figure 7-11. 7805 Schematic and Pin Layout

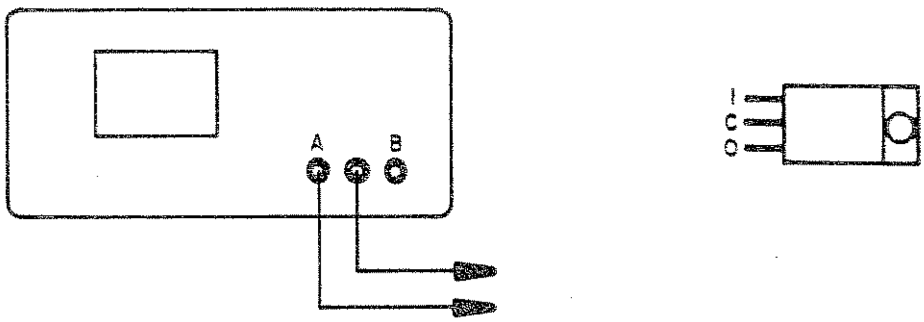
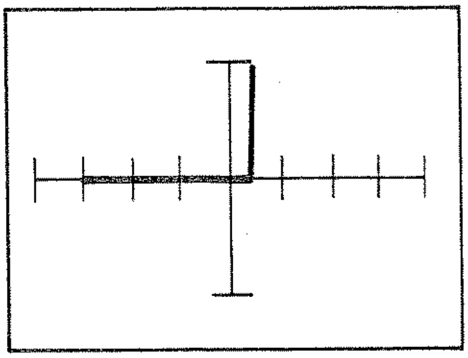
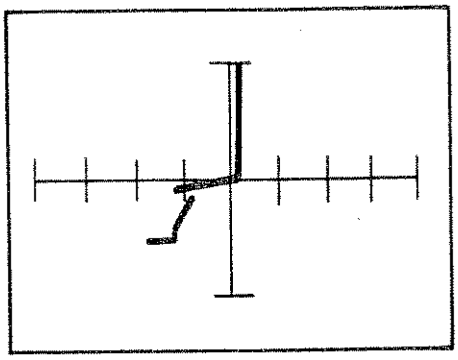


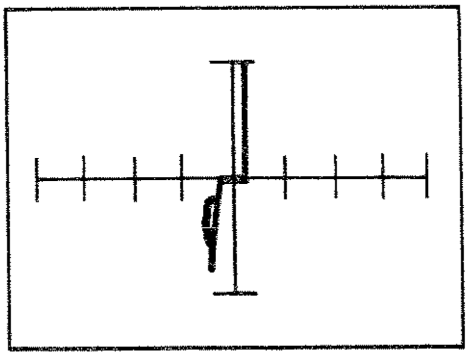
Figure 7-12. Test Connections to a 7805 +5V Regulator



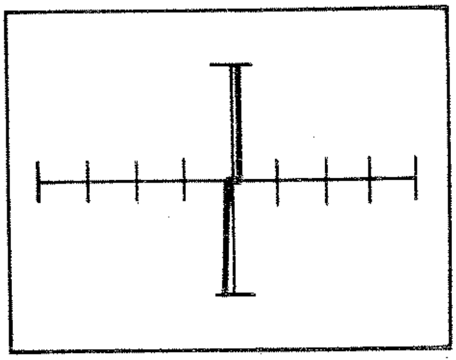
Low



Medium 1

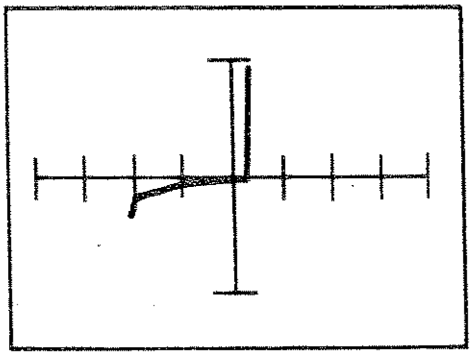


Medium 2

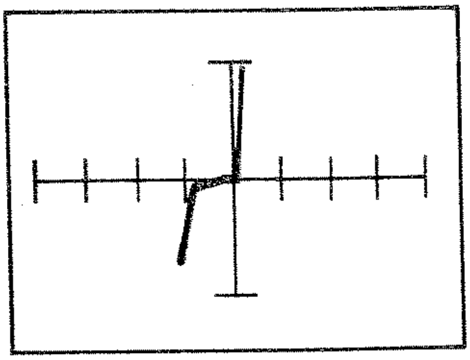


High

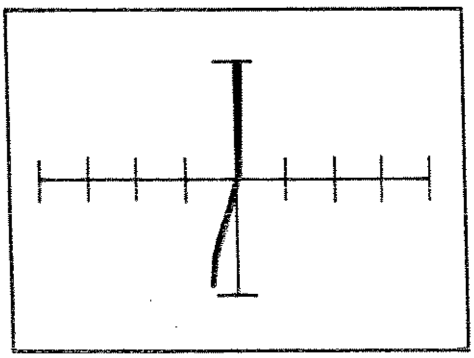
Figure 7-13. Signatures Between The Input and Ground Pins — 7805 at 60Hz



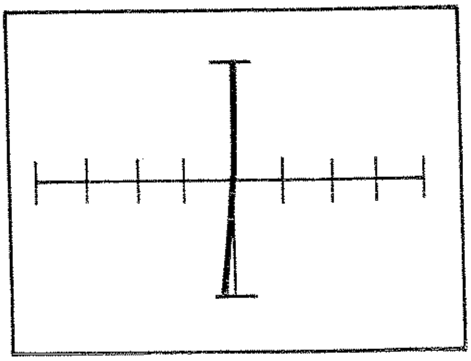
Low



Medium 1



Medium 2



High

Figure 7-14. Signatures Between The Output and Ground Pins — 7805 at 60Hz

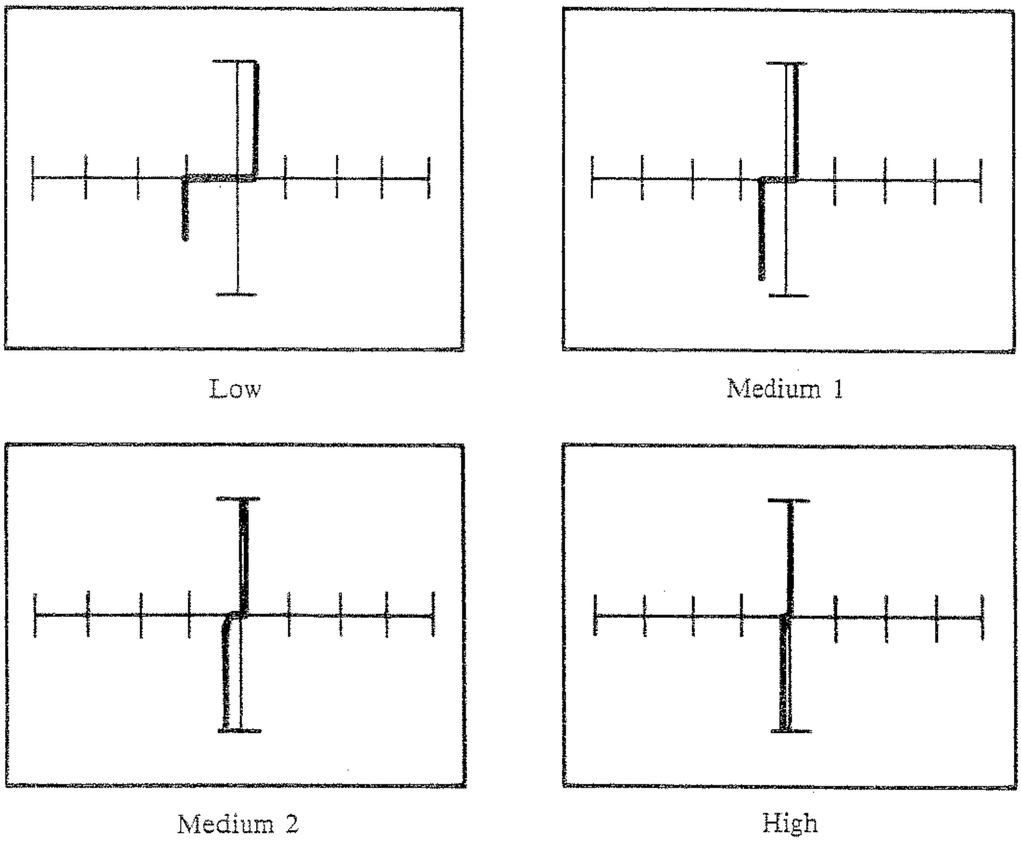


Figure 7-15. Signatures Between The Input and Output Pins — 7805 at 60Hz

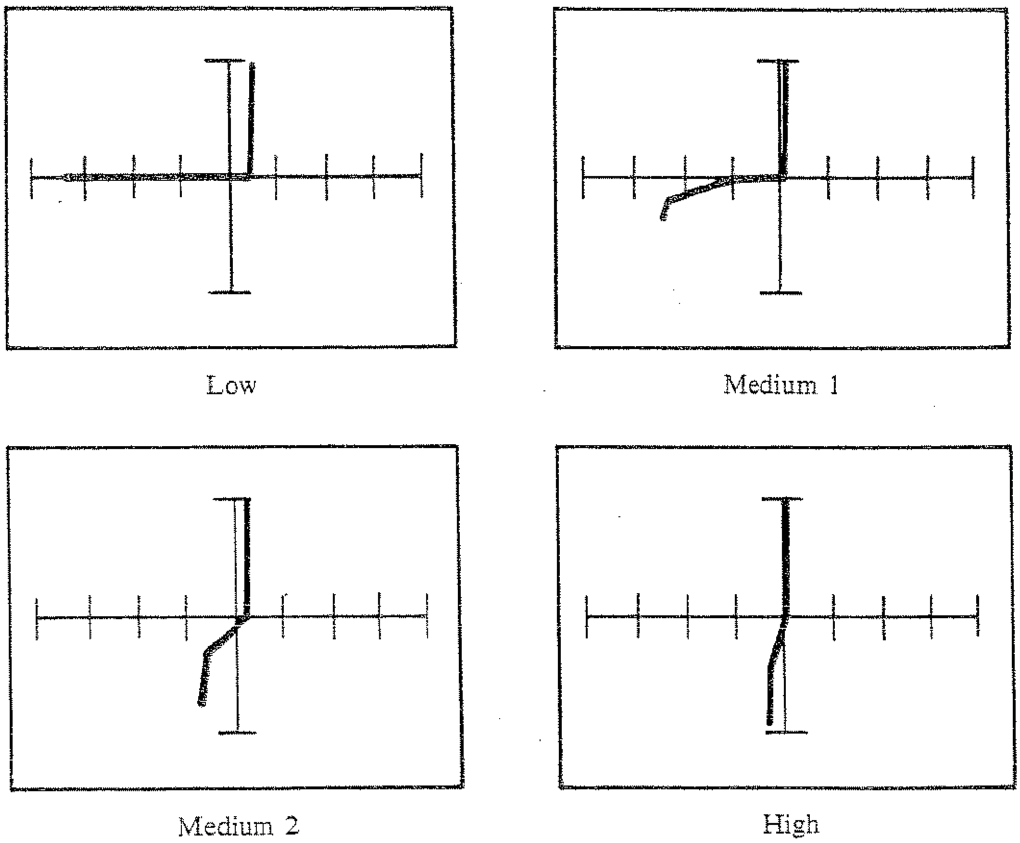


Figure 7-16. Signatures Between The Input and Output Pins of a Defective 7805 at 60Hz

7.3.2 The 7905 Regulator

Figure 7-17 shows the schematic and connection diagrams for a 7905 −5V regulator. Figure 7-18 shows the test connections to the 7905 voltage regulator. Figures 7-19 through 7-21 show the test signatures for a 7905 voltage regulator on all ranges. Again, these signatures are for references only and change slightly from manufacturer to manufacturer.

Figure 7-22 shows the signatures of a defective 7905 voltage regulator. Comparing Figure 7-21 and Figure 7-22 in medium 1 range, there is a significant difference in signatures.

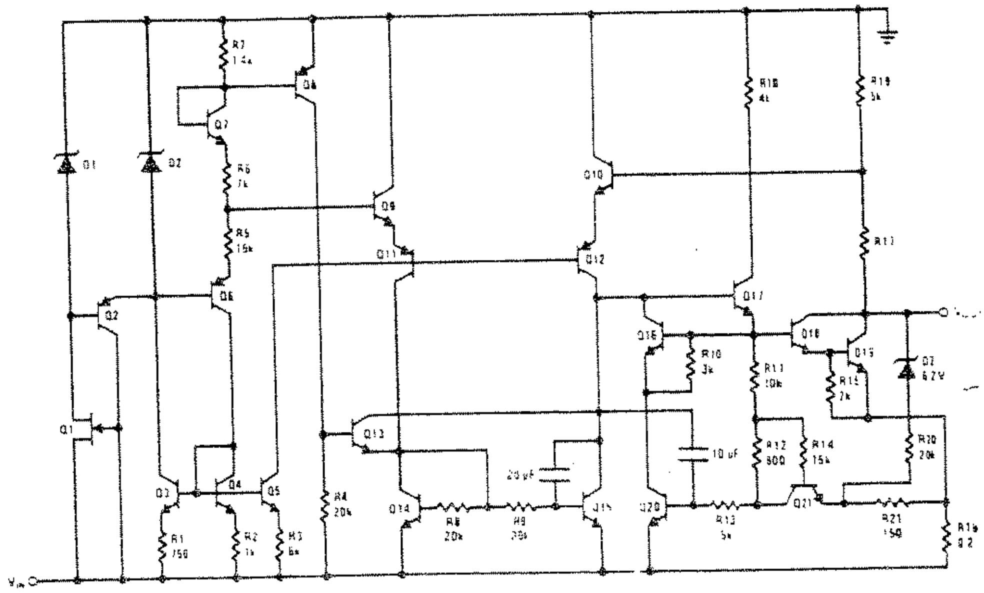


Figure 7-17. Schematic and Connections of the 7905 −5V Regulator

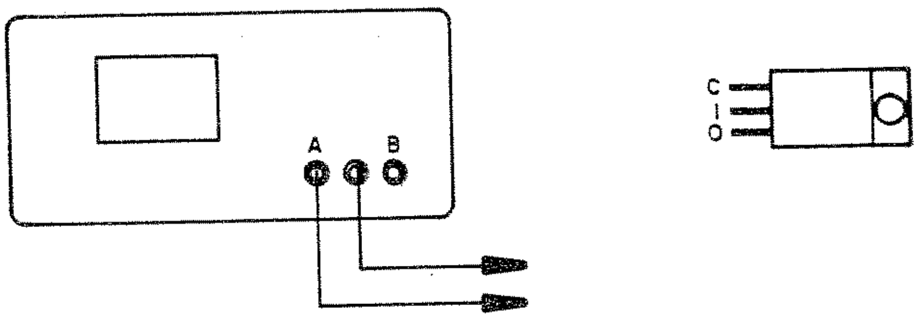
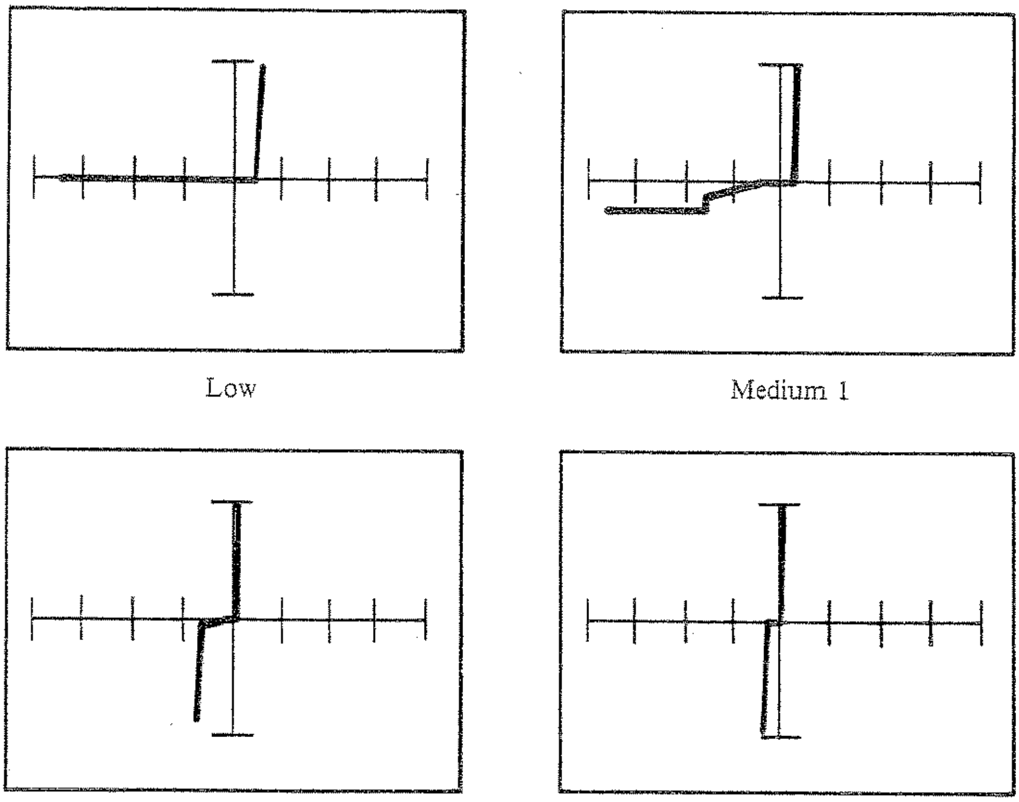


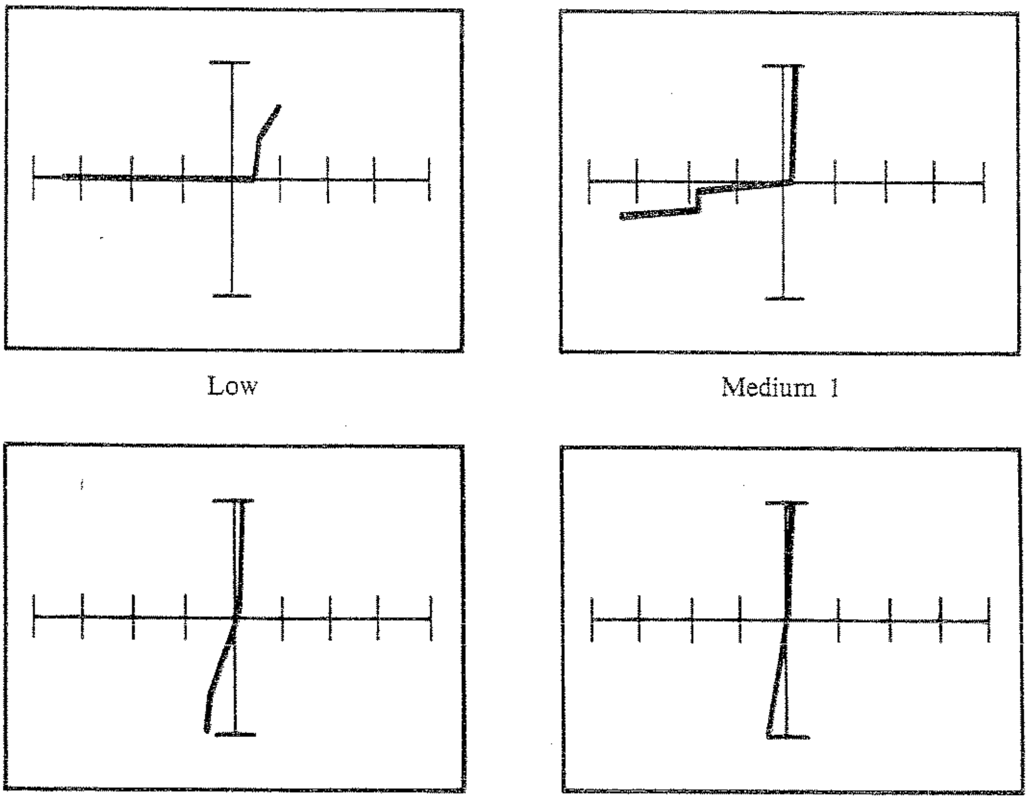
Figure 7-18. Test Connections to the 7905



Low Medium 1

Medium 2 High

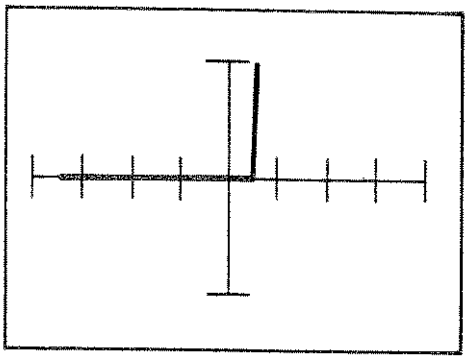
Figure 7-19. Signatures Between the Input and Ground Pins — 7905 at 60Hz



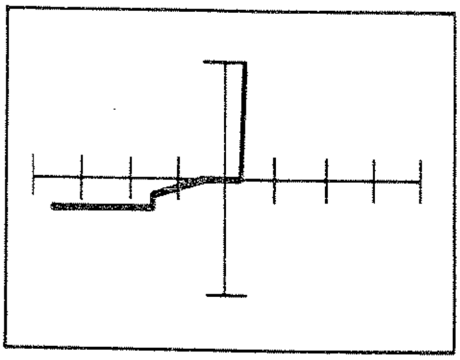
Low Medium 1

Medium 2 High

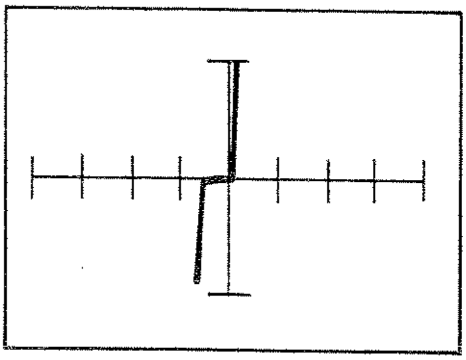
Figure 7-20. Signatures Between the Output and Ground Pins — 7905 at 60Hz



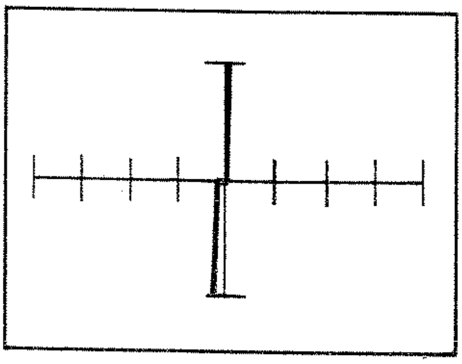
Low



Medium 1

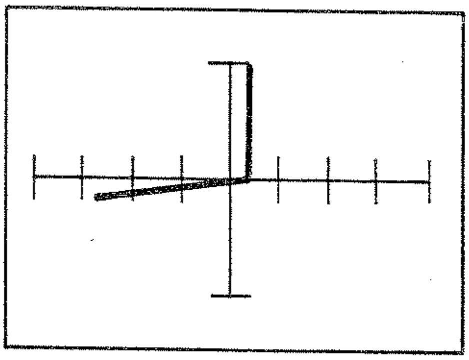


Medium 2

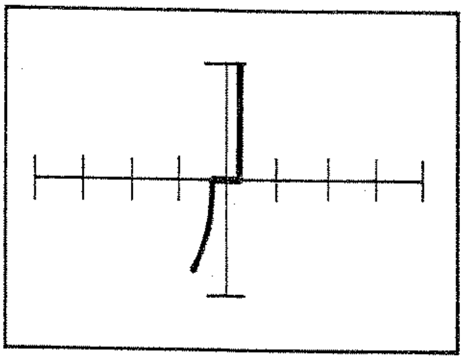


High

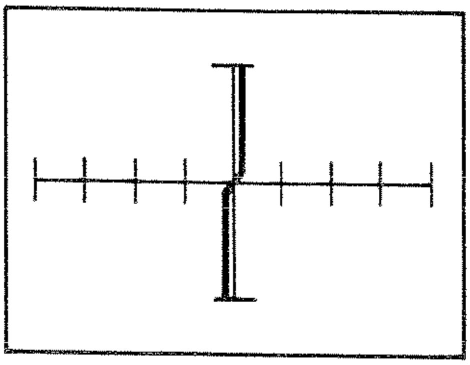
Figure 7-21. Signatures Between the Input and Output Pins — 7905 at 60Hz



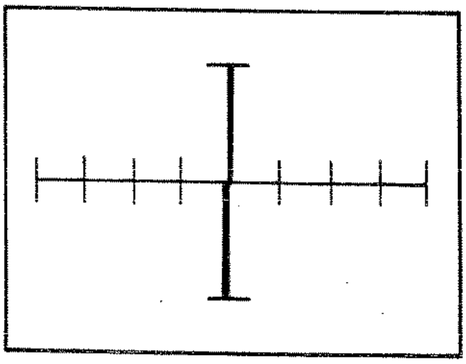
Low



Medium 1



Medium 2



High

Figure 7-22. Signatures Between the Input and Output Pins of a Defective 7905 at 60Hz

7.4 555 TIMERS

The 555 timer is a popular linear integrated circuit, and is used in precision timing, pulse generation, and pulse width modulation applications. The Tracker 2000 is used to examine signatures between various pins with respect to ground. Figure 7-23 shows the schematic and connection diagram of the National Semiconductor LM555 timer. Figure 7-24 shows the test connections of the LM555 to the Tracker 2000.

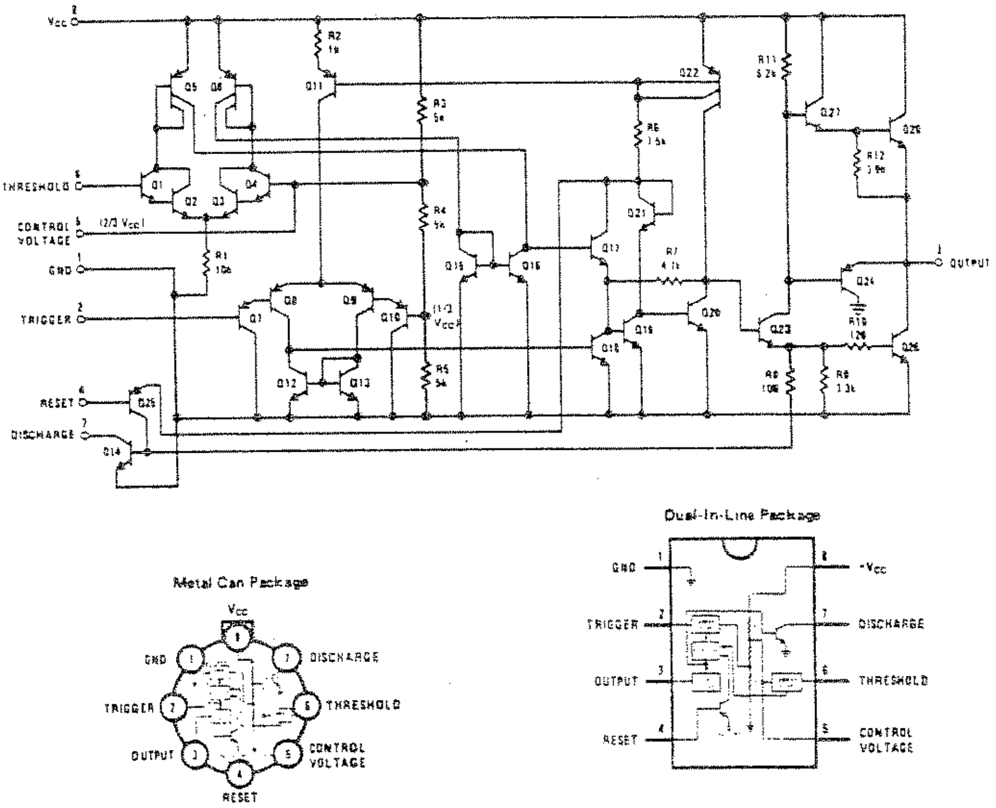


Figure 7-23. Schematic and Connection Diagram of an LM555 Timer

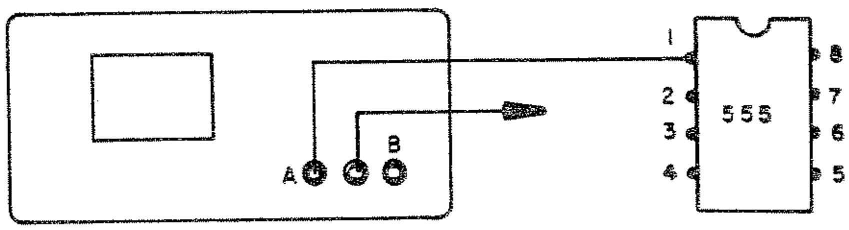


Figure 7-24. Test Connections to the LM555 Timer

Figures 7-25 through 7-28, and 7-30 through 7-33, show the signatures between different pins of the M555 using all ranges of the Tracker 2000. In Figure 7-25 the Tracker 2000 displays the base-collector nction of transistor Q7 (see schematic in Figure 7-23).

Figure 7-27 shows the signatures between Pin 4 (reset) and Pin 1 (gnd). In this case, the Tracker 2000 displays the series junctions of transistors Q25 and Q14 (see Figure 7-23). Consequently, a transistor signature is expected.

Figure 7-28 shows the signatures between Pin 5 (control voltage) and Pin 1. Pin 5 is connected to resistors R3, R4, R5, and the Darlington transistor formed by Q3 and Q4. Refer also to Figure 7-29. The impedance between pin 5 and pin 1 is too high to cause any significant effect in low range. As a result, a horizontal line is produced.

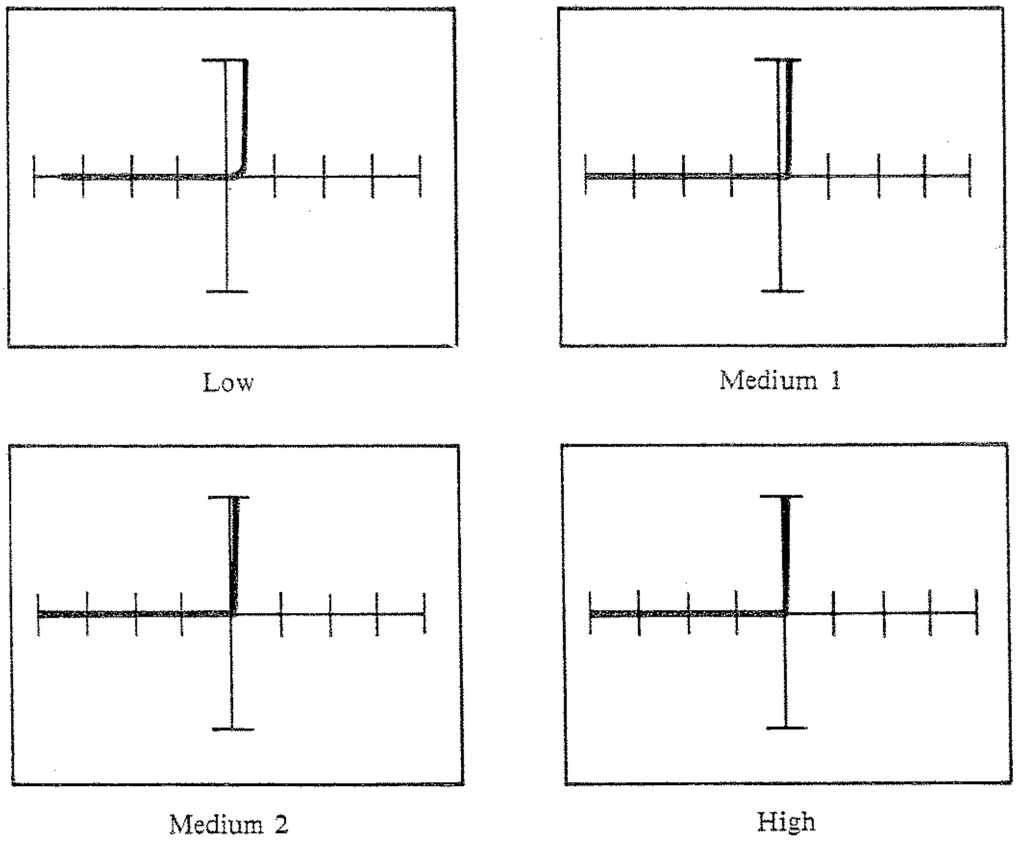


Figure 7-25. Signatures Between Pin 2 and Pin 1 of an LM555 Timer at 60Hz

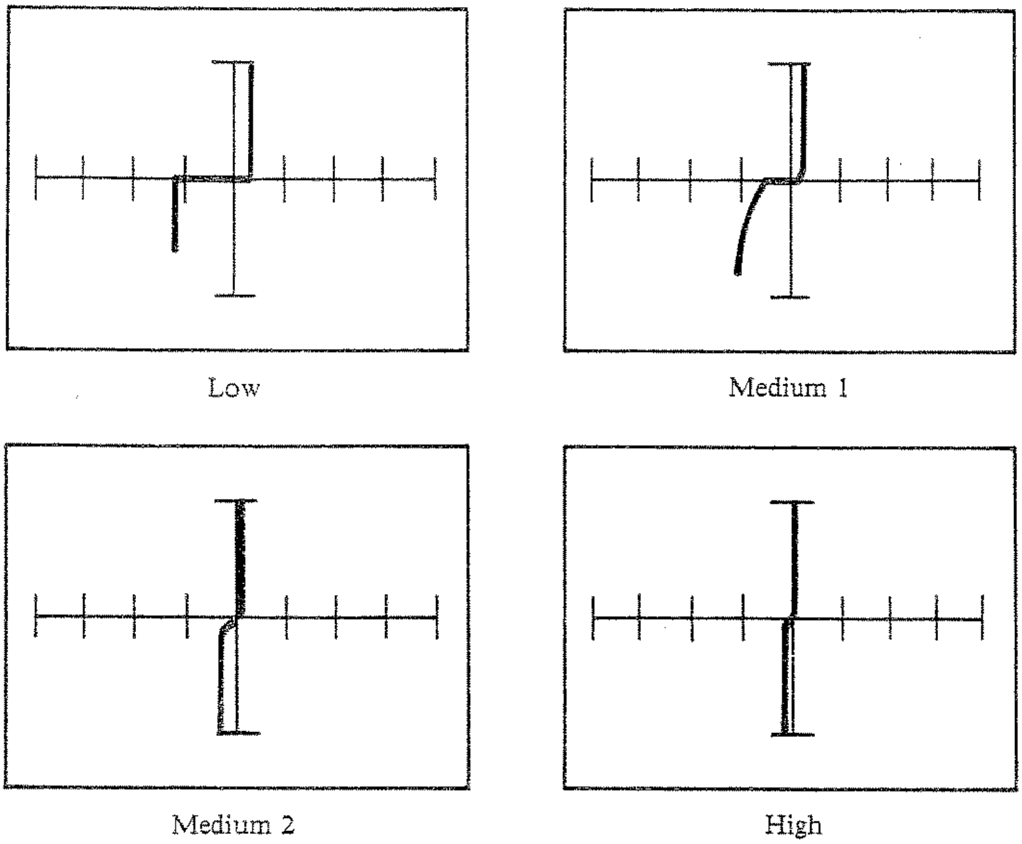


Figure 7-26. Signatures Between Pin 3 (Output) and Pin 1 of an LM555 Timer at 60Hz

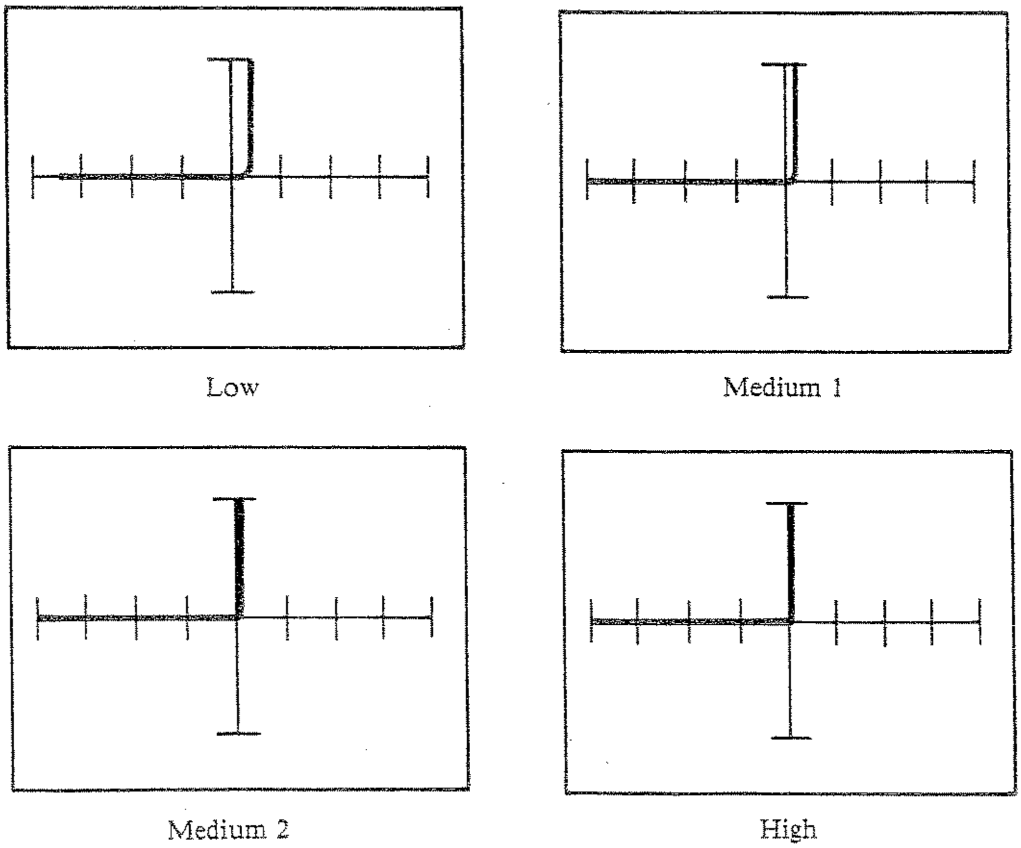


Figure 7-27. Signatures Between Pin 4 (Reset) and Pin 1 of an LM555 Timer at 60Hz

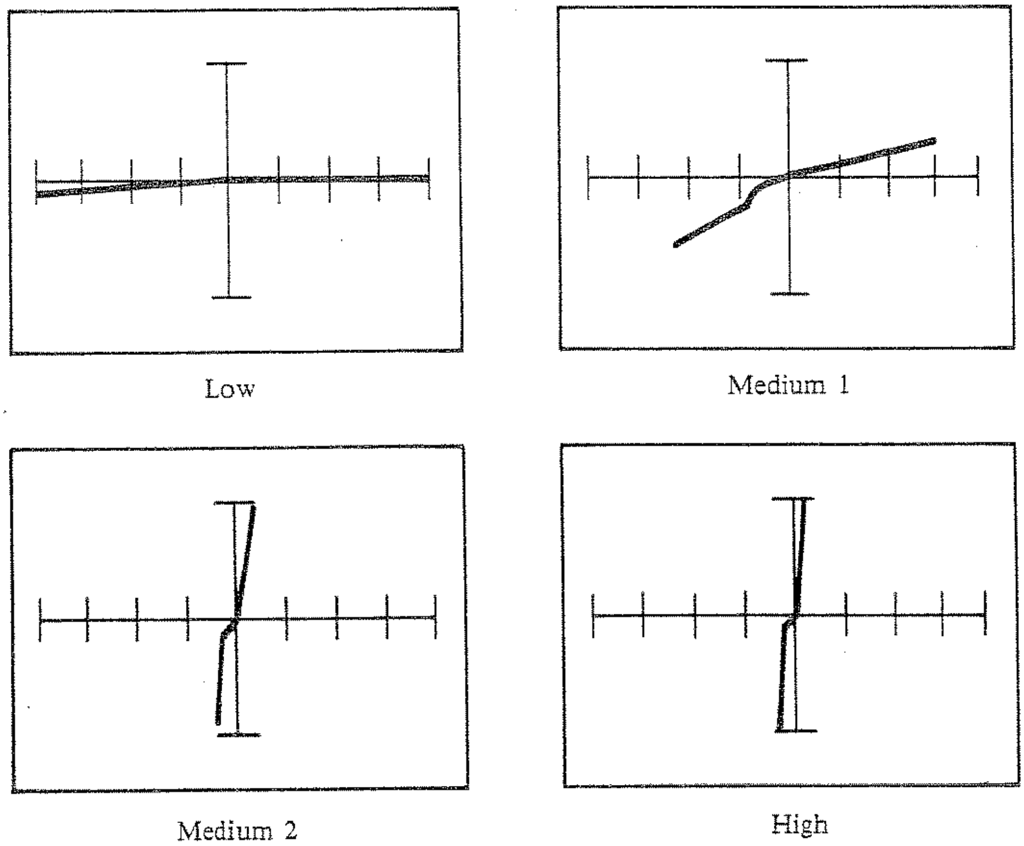


Figure 7-28. Signatures Between Pin 5 (Control Voltage) and Pin 1 of an LM555 Timer at 60Hz

Figure 7-30 shows the signatures between pin 6 and pin 1. Pin 6 is connected to a Darlington transistor (formed by Q1 and Q2) which is in series with resistor R1 (10k resistor). The impedance is too high to show much change in the low range.

Figure 7-31 shows the signatures between pin 7 and pin 1. These pins are connected to the collector and emitter of Q14.

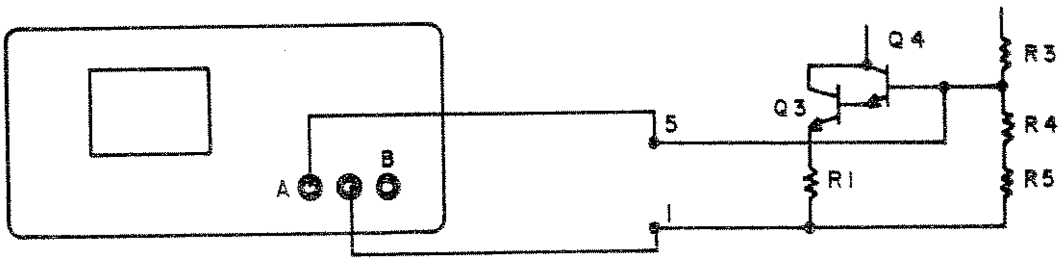


Figure 7-29. Test Connections of an LM555 Pin 1 and Pin 5

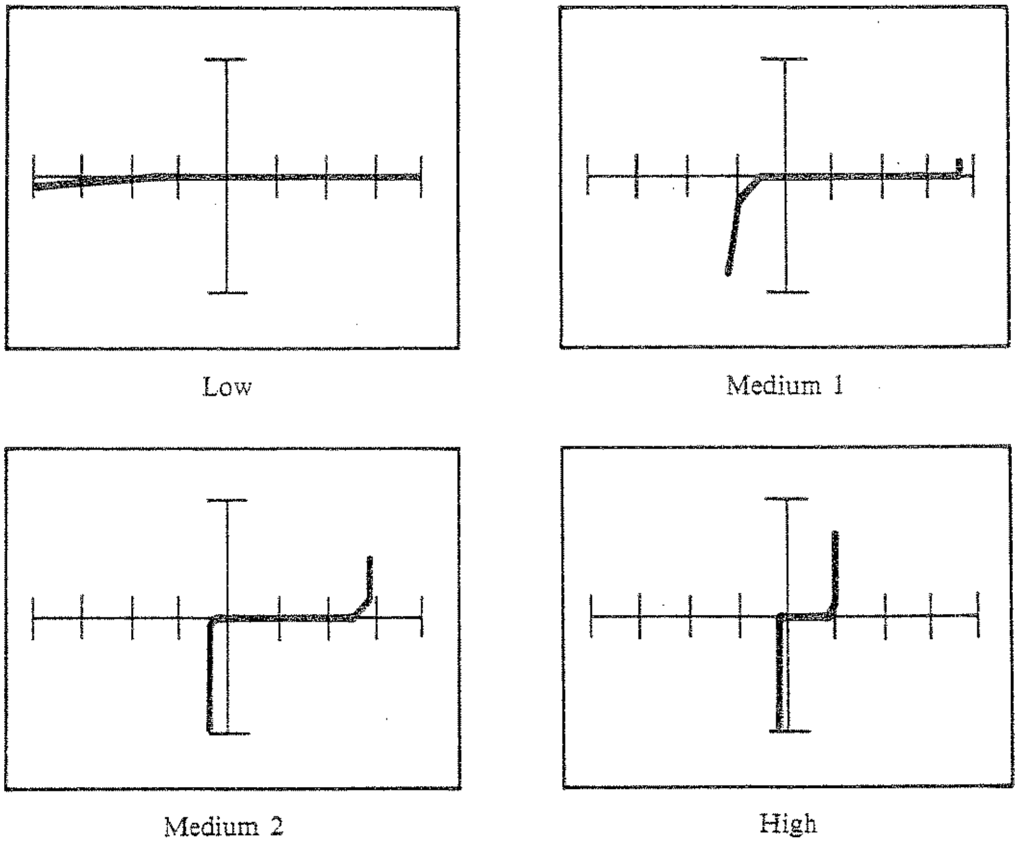


Figure 7-30. Signatures Between Pin 6 (Threshold) and Pin 1 of an LM555 Timer at 60Hz

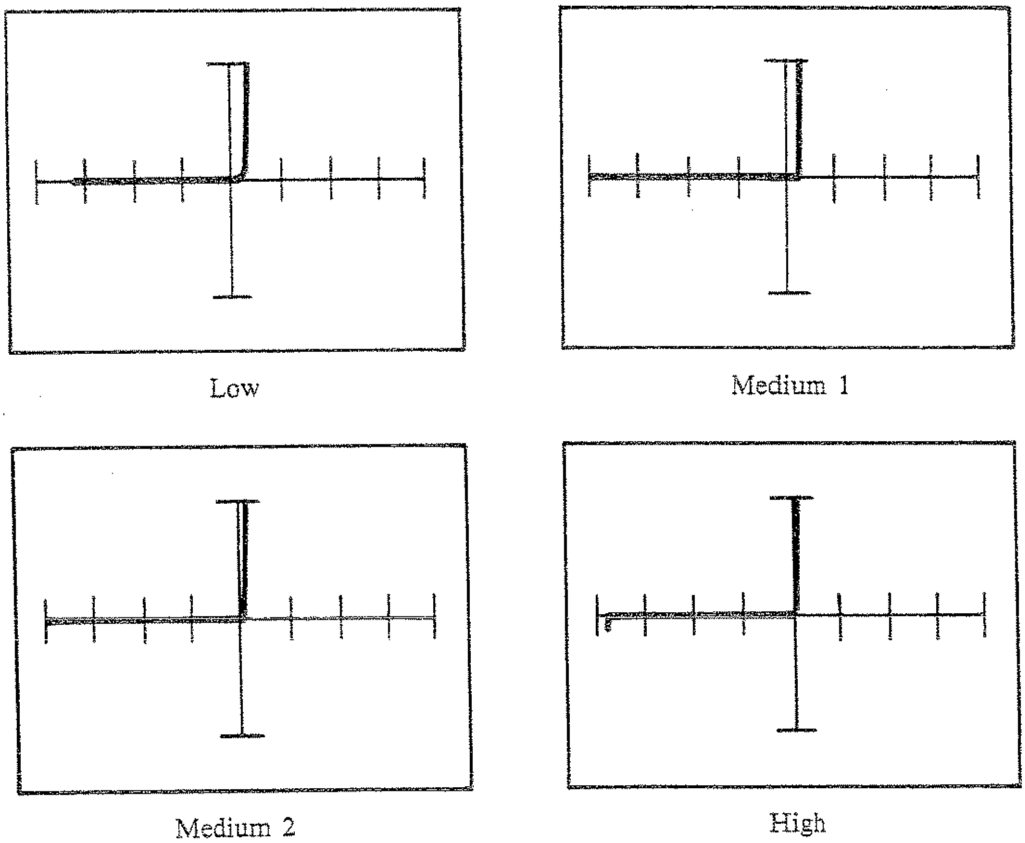


Figure 7-31. Signatures Between Pin 7 (Discharge) and Pin 1 of an LM555 Timer at 60Hz

Figure 7-32 shows the signatures between Pin 8 (V_{CC}) and Pin 1. Figure 7-33 shows the signature between the same pins of an LM555 timer which was damaged by power supply polarity reversal.

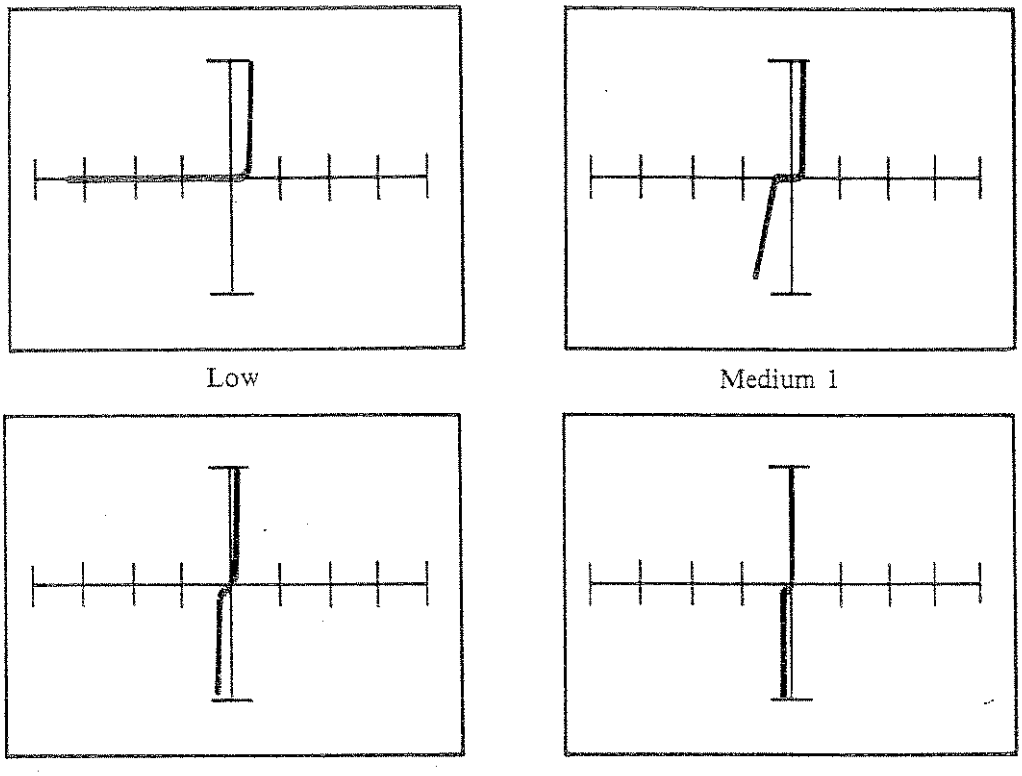


Figure 7-32. Signatures Between Pin 8 (V_{CC}) and Pin 1 of an LM555 Timer at 60Hz.

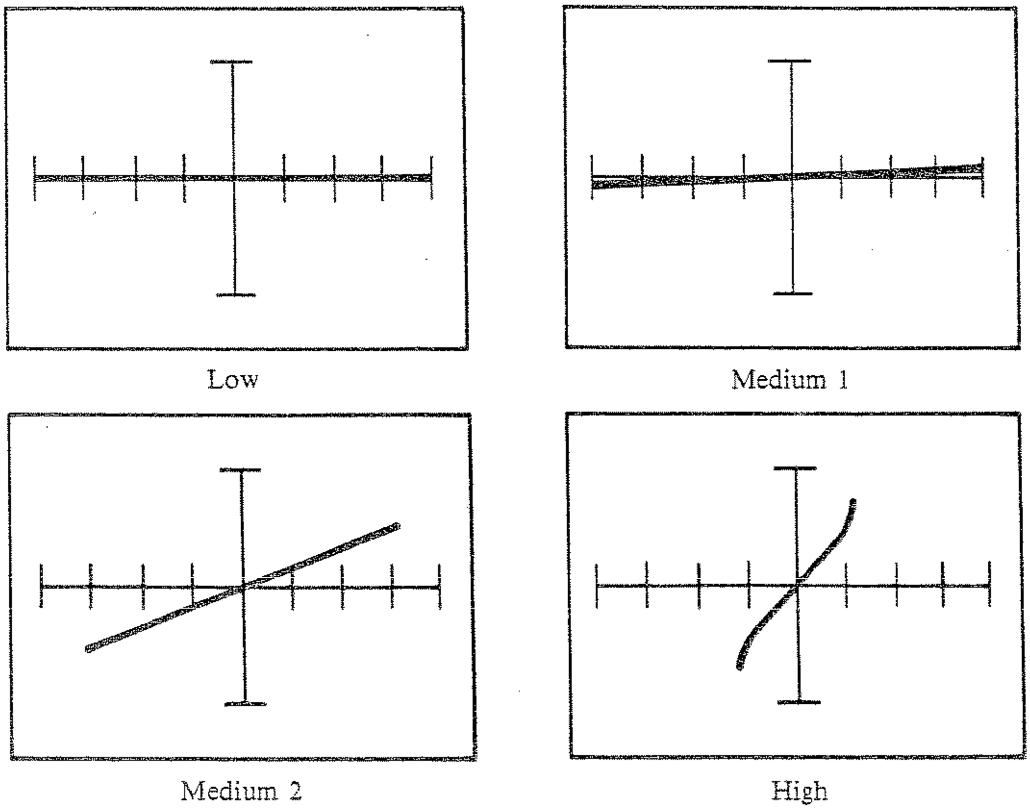


Figure 7-33. Signatures Between Pin 8 (V_{CC}) and Pin 1 of a Damaged LM555 Timer at 60Hz.

7.5 TTL DIGITAL INTEGRATED CIRCUITS

7.5.1 General

The schematics of the basic gates of the various families are shown in Figures 7-34a, b, c, d, and e. All are similar, containing an input, gate, phase splitter (Q2) with emitter and collector load resistors, pull-up mechanism (Q3 / Q4) and a pull-down transistor (Q5). In all TTL circuits, except LS TTL circuits, the AND function is formed by a multi-emitter transistor in which the emitter-base junctions serve to isolate the input signal sources from each other.

The inputs of these gates contain input protection diodes. To test a digital IC, we need to examine:

- Inputs with respect to ground to see if the input diode and transistor are damaged.
- Output pin with respect to ground to see if the C-E junction of Q5 is damaged.
- Output pin with respect to V_{cc} to see if Q4 is damaged.
- V_{cc} with respect to ground. Generally, the Tracker 2000 can display flaws caused by overloading.

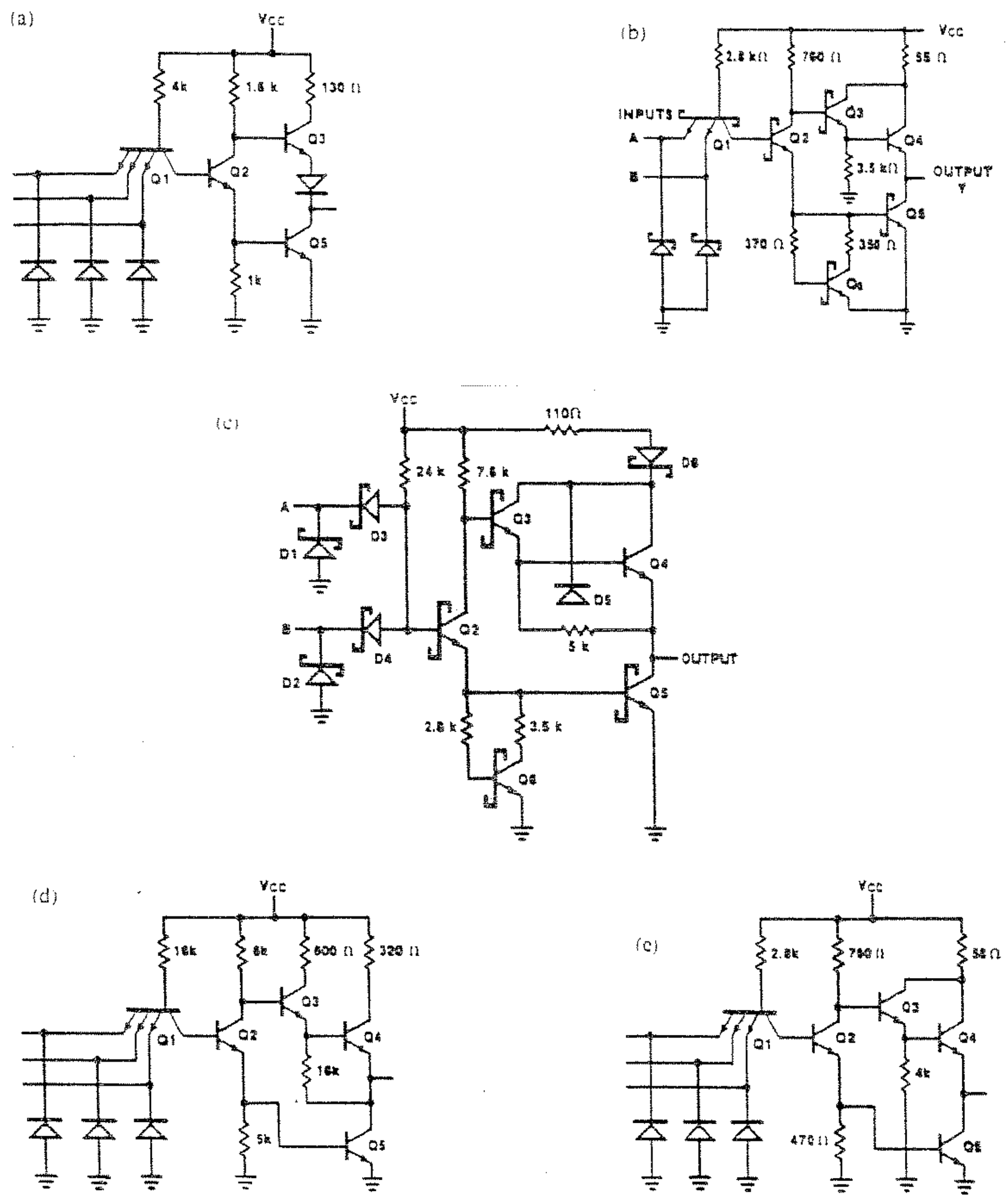


Figure 7-34. Various TTL Implementations

7.5.2 TTL Devices With Totem Pole Output

Figure 7-35 shows the Tracker 2000 test connections to a 7410 NAND gate. Figures 7-36 through 7-38 show the signatures of input, output, and V_{CC} with respect to ground of the 7410 TTL device. As mentioned previously, the test signatures may vary from device to device, and from manufacturer to manufacturer, depending on the level of doping and logic implementation.

Figure 7-36 shows the signatures between an input pin and the ground pin. In the low range, the input protection diode signature is represented by XYZ instead of WYZ (as a regular diode would have been represented). The difference between a regular diode and a protection diode is that protection diodes have a 50 ohm resistance in series with the diode junction.

Figure 7-37 shows the signatures between an output pin and the ground pin. In low range, the test voltage is not high enough to cause non-destructive breakdown.

Figure 7-38 shows the signatures between the V_{CC} pin and the ground pin.

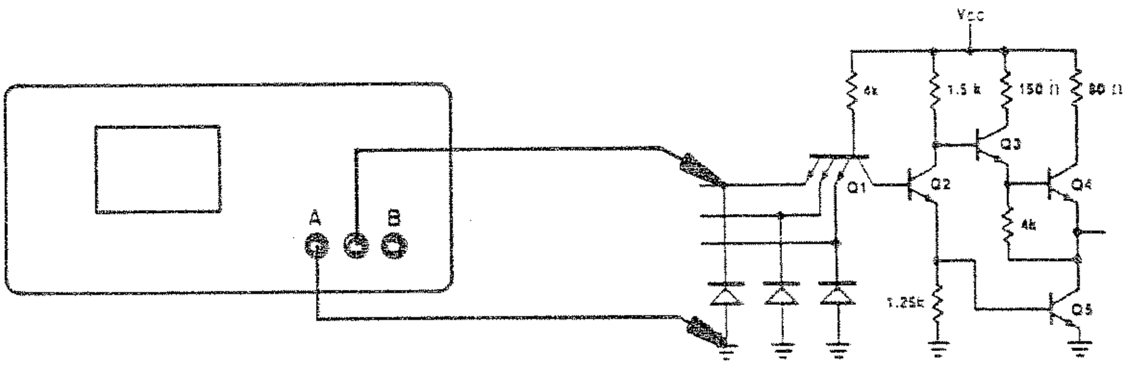
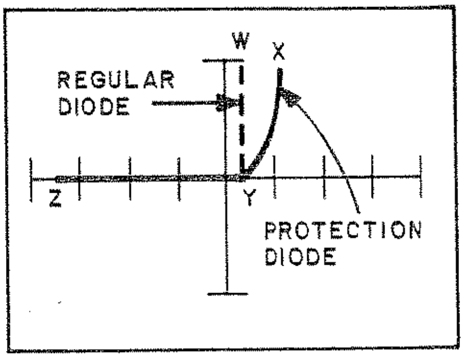
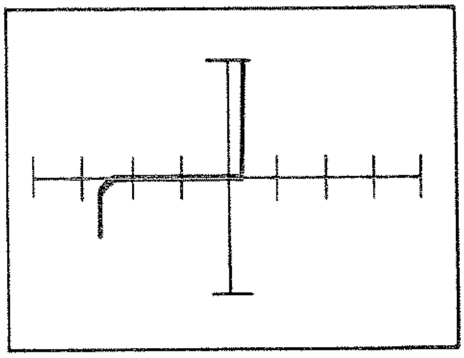


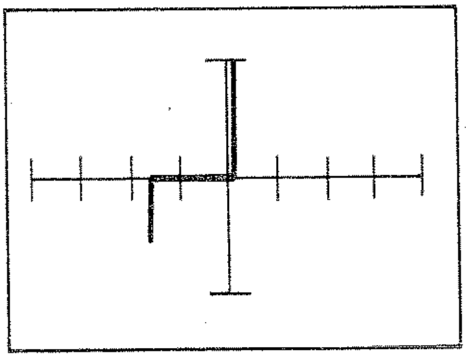
Figure 7-35. Test Circuit for the 7410 NAND Gate



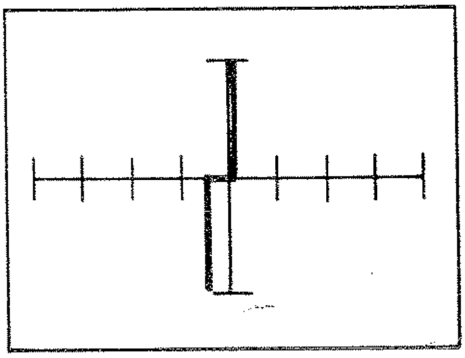
Low



Medium 1

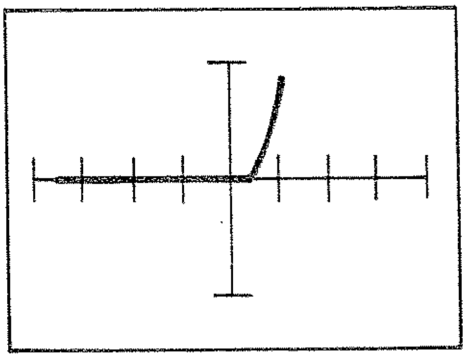


Medium 2

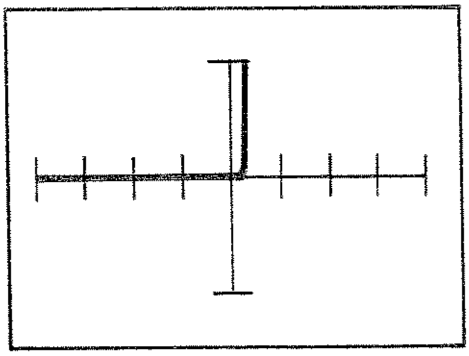


High

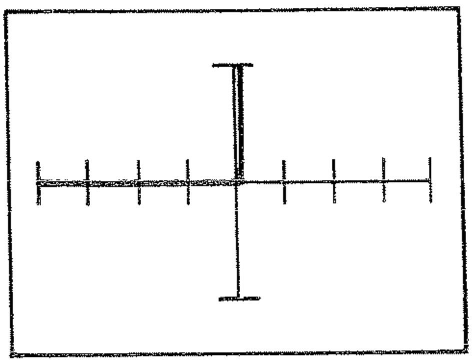
Figure 7-36. Signatures Between an Input Pin and Ground Pin of a 7410 at 60Hz



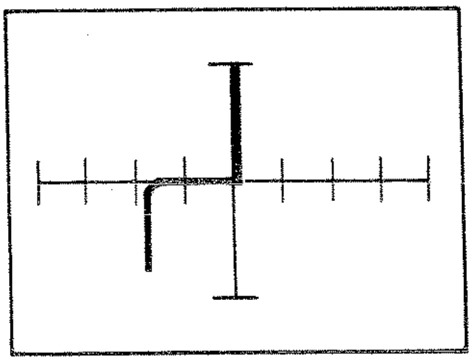
Low



Medium 1



Medium 2



High

Figure 7-37. Signatures Between an Output Pin and the Ground Pin of a 7410 at 60Hz

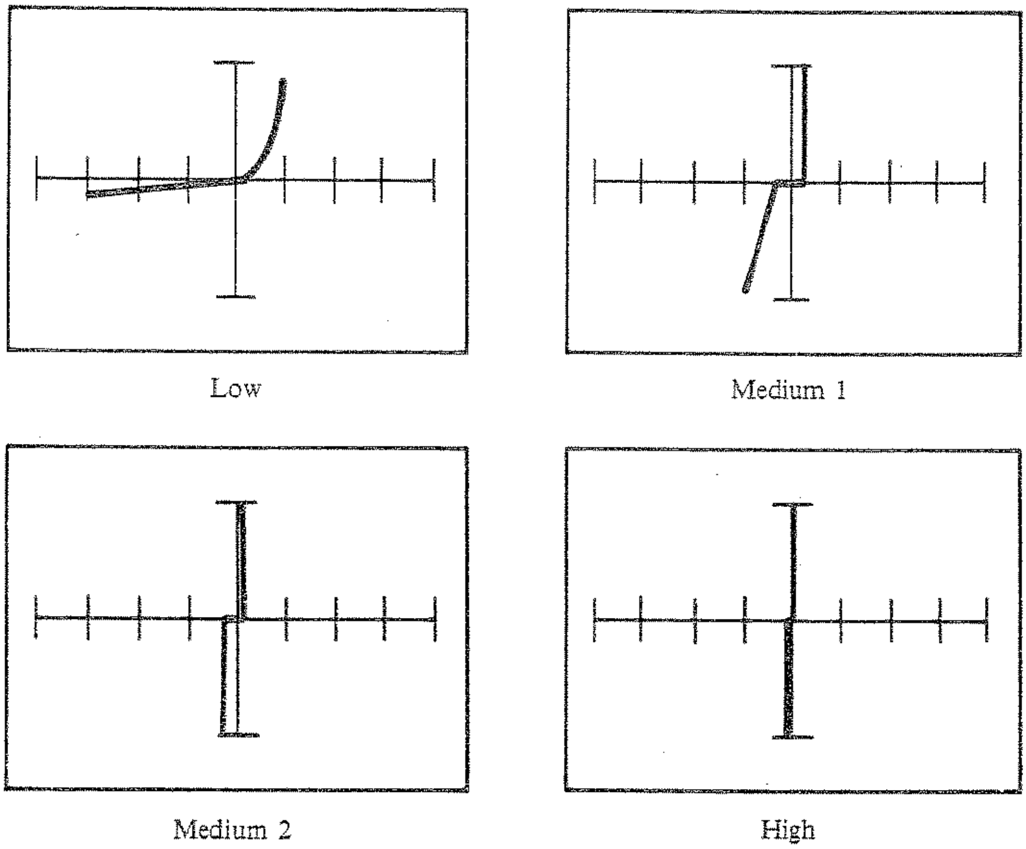
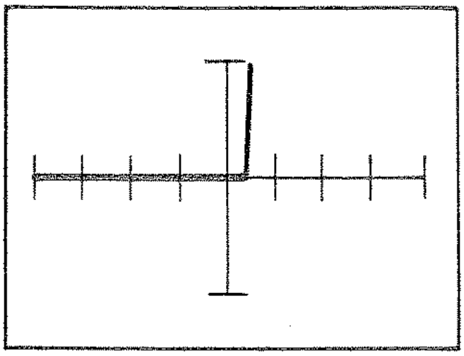


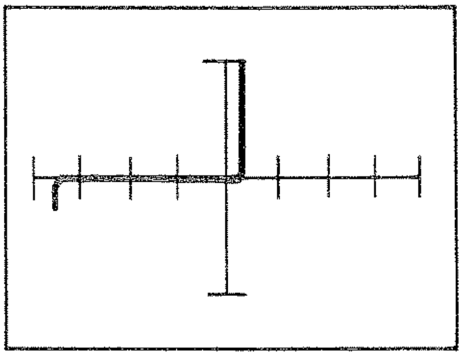
Figure 7-38. Signatures Between the V_{cc} Pin and Ground Pin of a 7410 at 60Hz.

7.5.3 LS TTL Devices

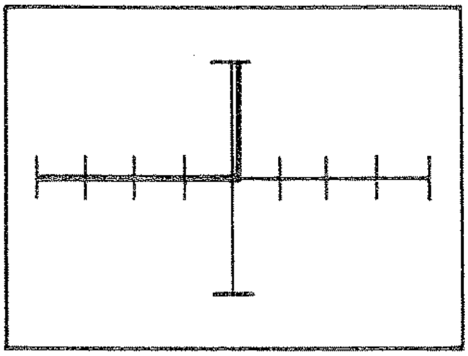
Implementation of LS digital ICs is different from others (refer to Figure 7-35). The LS series is not implemented with multiple-emitter transistor topology. Figures 7-39 through 7-41 show the signatures between different pins of a 74LS32.



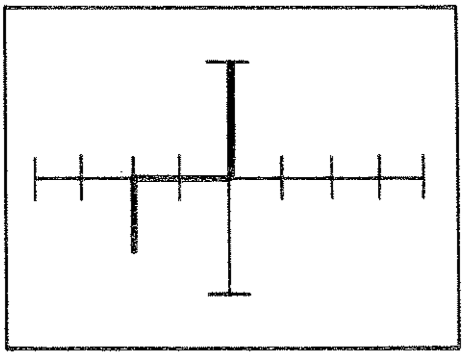
Low



Medium 1

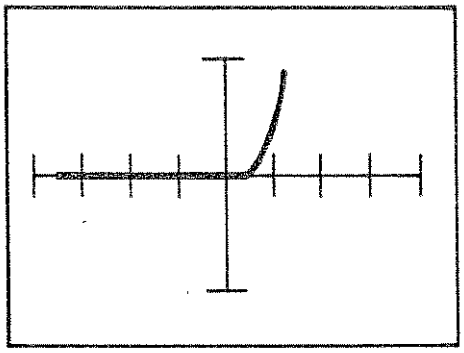


Medium 2

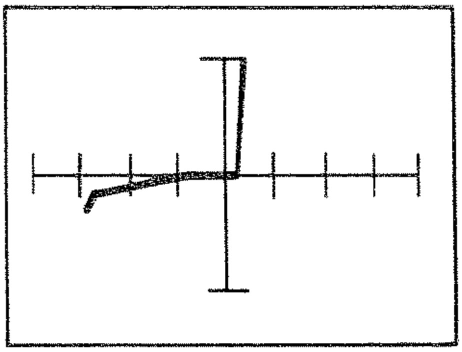


High

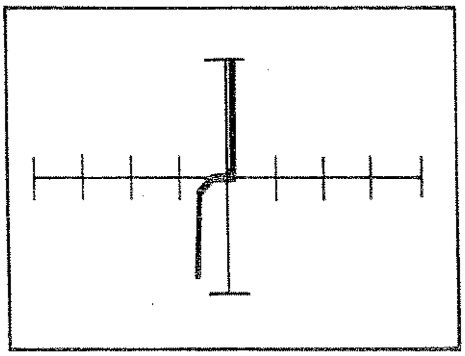
Figure 7-39. Signatures Between an Input Pin and the Ground Pin of a 74LS32 at 60Hz



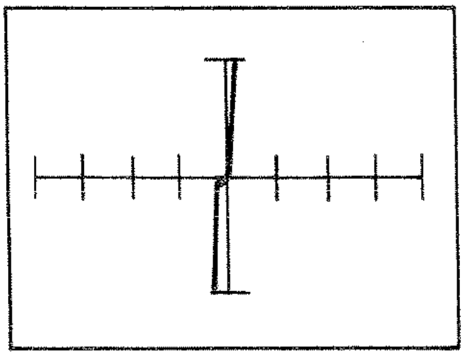
Low



Medium 1

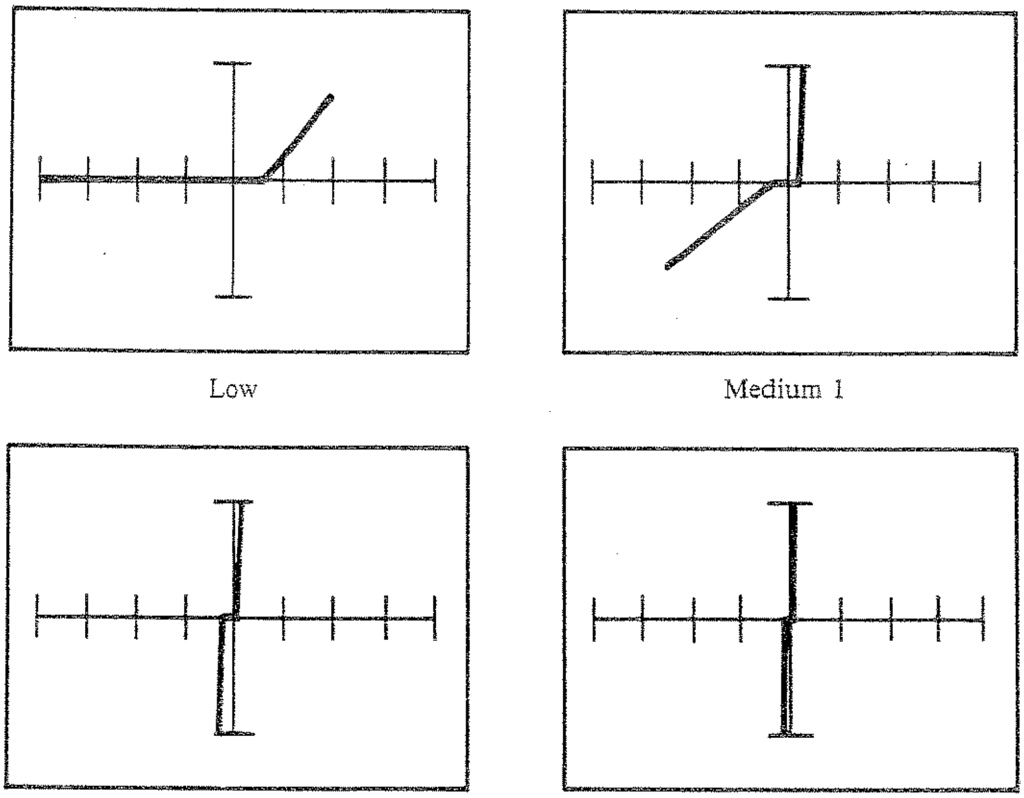


Medium 2



High

Figure 7-40. Signatures Between an Input Pin and Output Pin of a 74LS32 at 60Hz



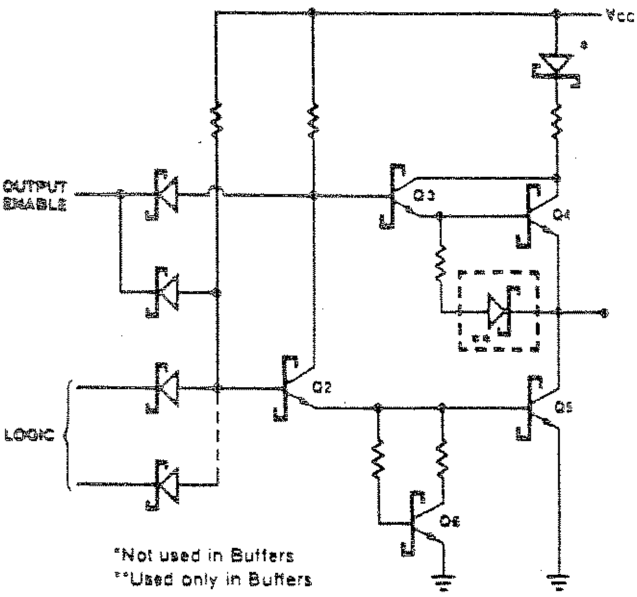
Low — Medium 1

Medium 2 — High

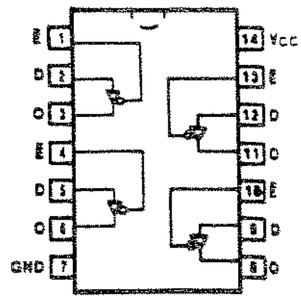
Figure 7-41. Signatures Between the V_{cc} Pin and Ground Pin of a 74LS32 at 60Hz

7.5.4 Tri-State LS TTL Devices

In the tri-state LS TTL family, there are many circuits that have an auxiliary control input that allows both the output pull-up and pull-down circuitry to be disabled. This condition is called the high impedance (high Z) state and allows the outputs of different circuits to be connected to a common line or data bus. Figure 7-42 shows a typical tri-state output device. The device to be tested has power off, so the enable pin is considered just another input pin, and tri-state devices are tested in the same manner as other TTL devices except their signatures are different. It is extremely easy to test a tri-state device when compared with a known-good device. Figure 7-43 shows a connection diagram of a 74LS125.

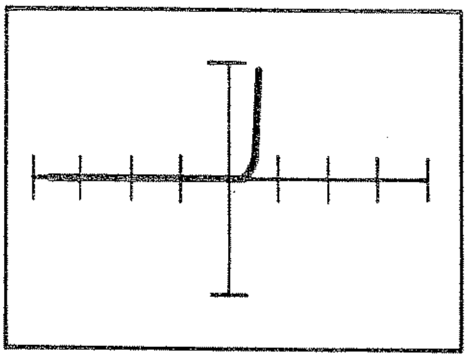


Typical Tri-State Output Control
Figure 7-42.

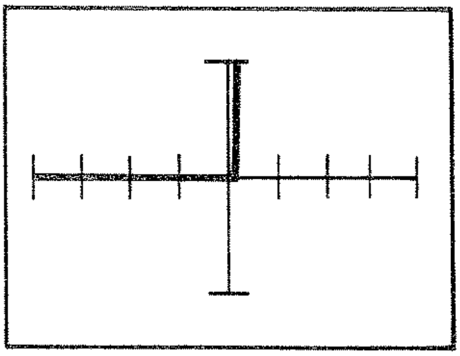


Connection Diagram
of a 74LS125
Figure 7-43.

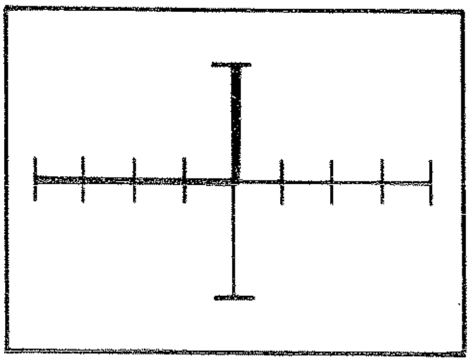
Figure 7-44 shows the signatures between an input pin and ground pin, and Figure 7-45 shows the signatures between the enable pin and ground pin. These two figures exhibit similar signatures because both the input and enable pins have similar electrical paths to ground.



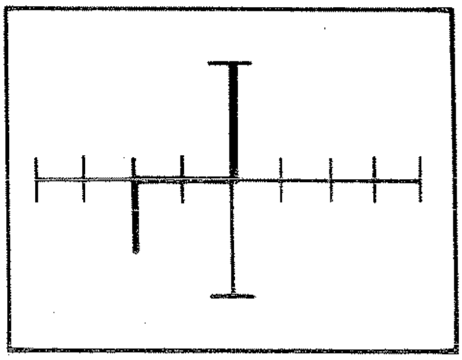
Low



Medium 1



Medium 2



High

Figure 7-44. Signatures Between an Input Pin and the Ground Pin of a 74LS125 at 60Hz

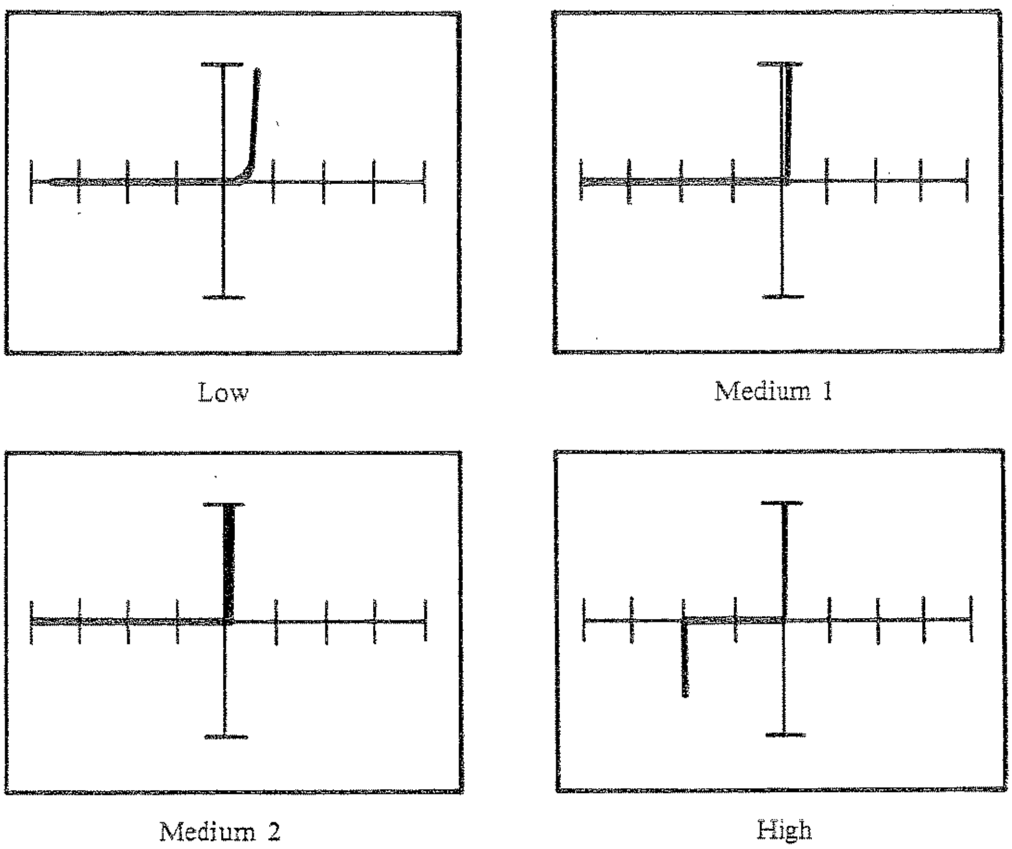


Figure 7-45. Signatures Between the Enable Pin and Ground Pin of a 74LS125 at 60Hz

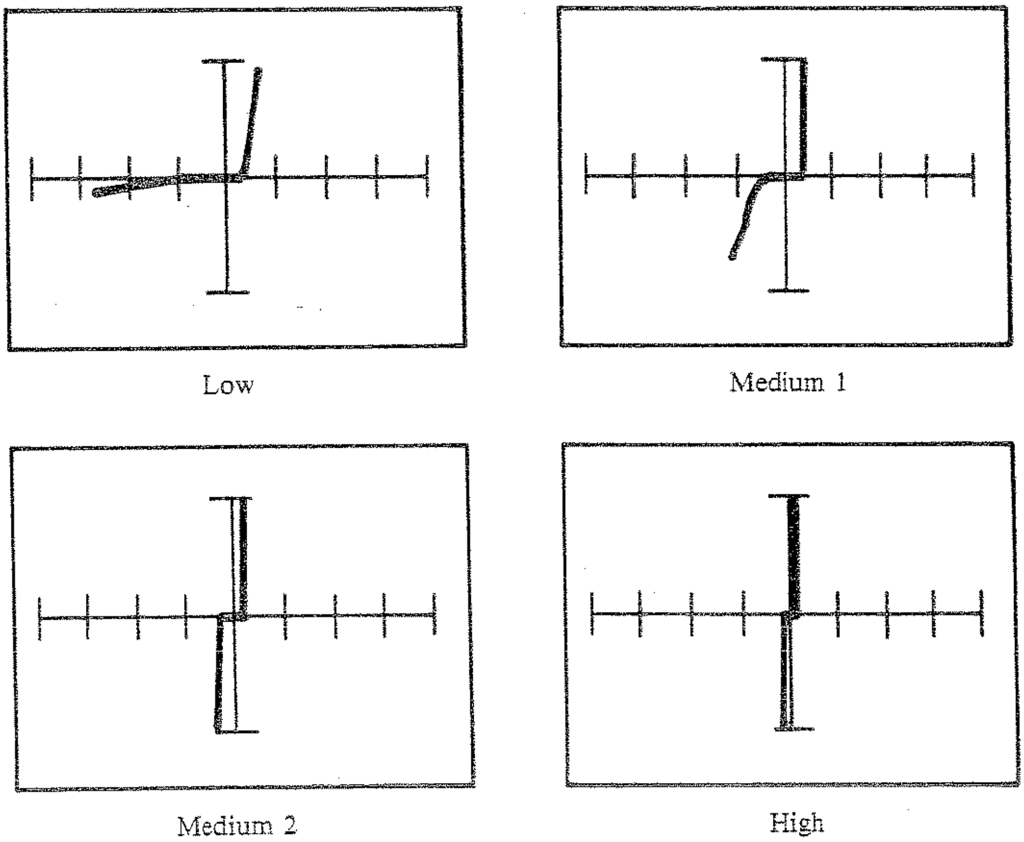


Figure 7-46. Signatures Between the V_{cc} Pin and Ground Pin of a 74LS125 at 60Hz.

7.6 CMOS INTEGRATED CIRCUITS

CAUTION

WHEN TESTING CMOS COMPONENTS BE SURE TO FOLLOW ALL STATIC HANDLING PRECAUTIONS. THESE INCLUDE:
- Store and transport in conductive packaging.
- The person handling the device should be grounded with a one Megohm wrist strap.
- All surfaces should be conductive and connected to earth ground.
- All parts should be handled by their packages and not by the leads.

THESE ARE SOME OF THE MAJOR PRECAUTIONS — CHECK THE MANUFACTURER'S HANDLING TECHNIQUES FOR COMPLETE PROCEDURES.

NOTE: When testing CMOS devices, it is recommended that the V_{ss} and V_{dd} pins be shorted together to eliminate noise in the Tracker 2000 signatures.

NOTE: Tests were conducted in an independent laboratory to show that the Tracker test signals are safe to test CMOS, MOS and low power Schottky devices. Refer to the Appendixes at the back of this manual.

The CMOS IC has become very popular because of its low power consumption and high noise immunity. Figure 7-47 shows the schematic and connection diagram of a Motorola MC14011B CMOS NAND gate. All CMOS input pins have protection diodes which have fairly high DC resistance. Figures 7-48 through 7-50 show the Tracker 2000 signatures between different pins of the MC14011B.

Figure 7-48 shows the signatures between an input pin and the ground pin of the MC14011B. In the low range, the signature does not look like that of a regular diode because of the high input resistance in series with the protection diodes.

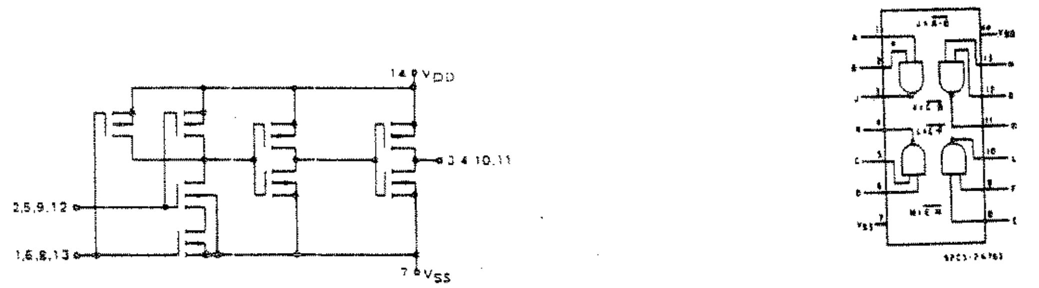


Figure 7-47. Schematic and Connection Diagram of a MC14011B

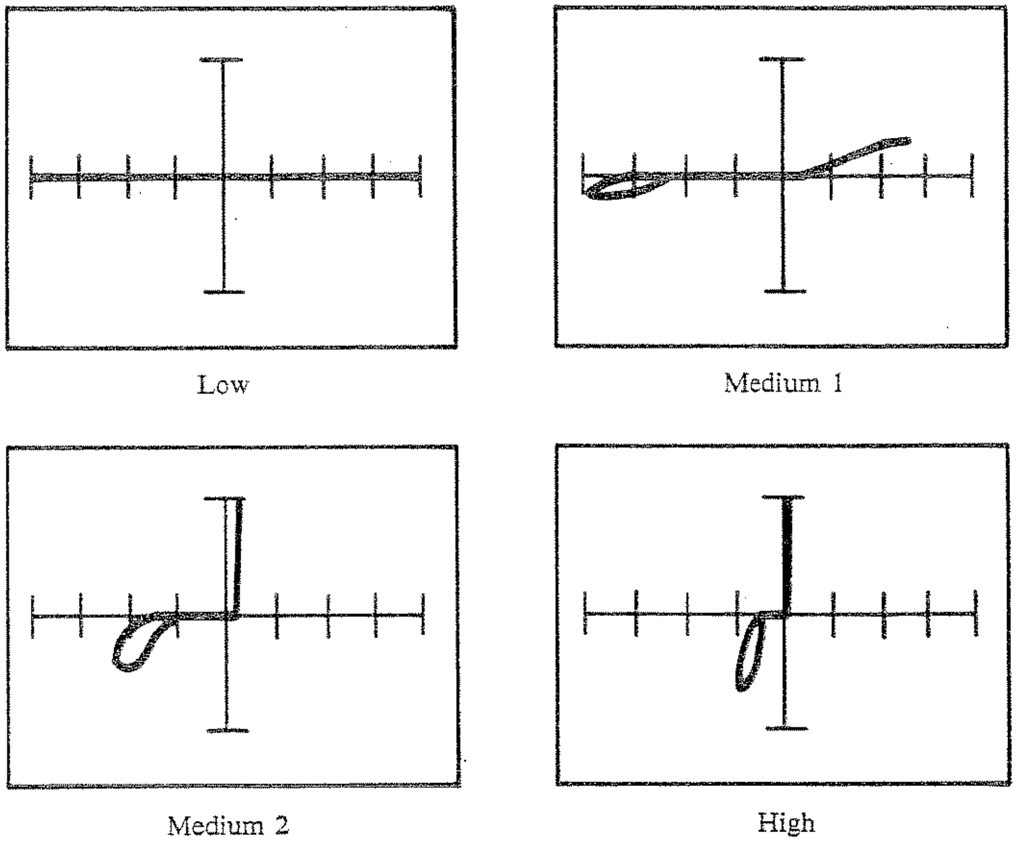


Figure 7-48. Signatures Between an Input Pin and the V_{ss} Pin of a MC14011B at 60Hz

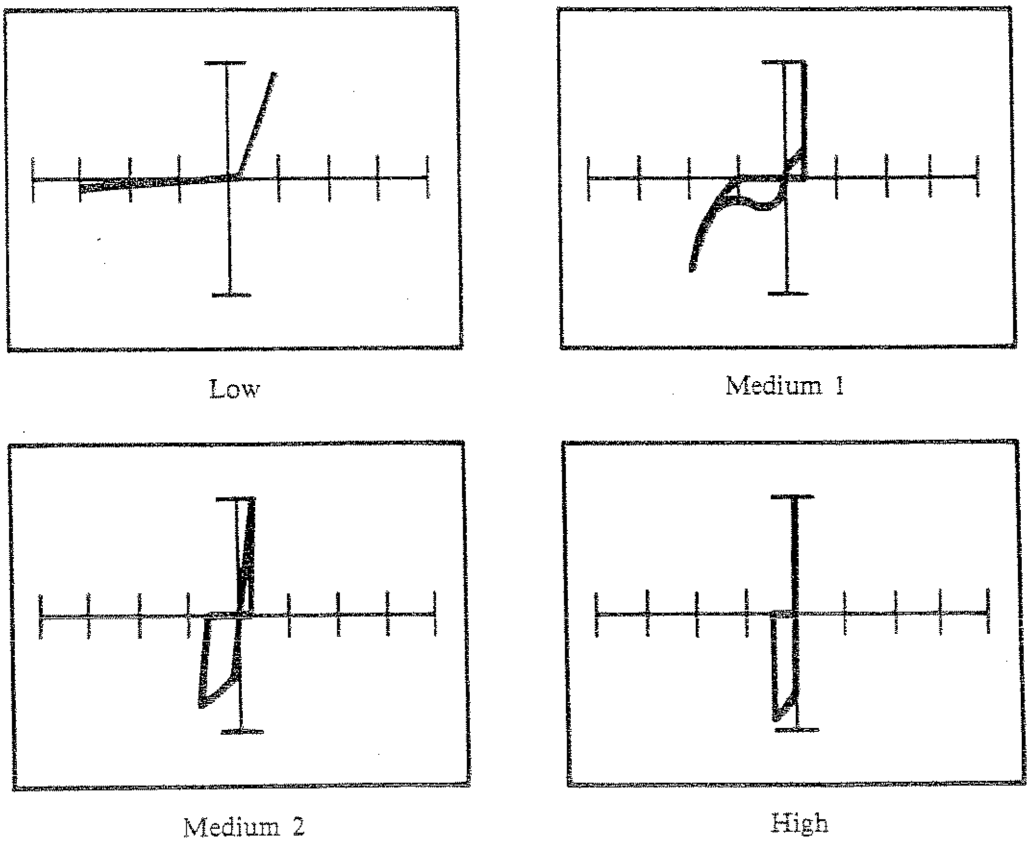


Figure 7-49. Signatures Between an Output Pin and V_{ss} Pin of a MC14011B at 60Hz

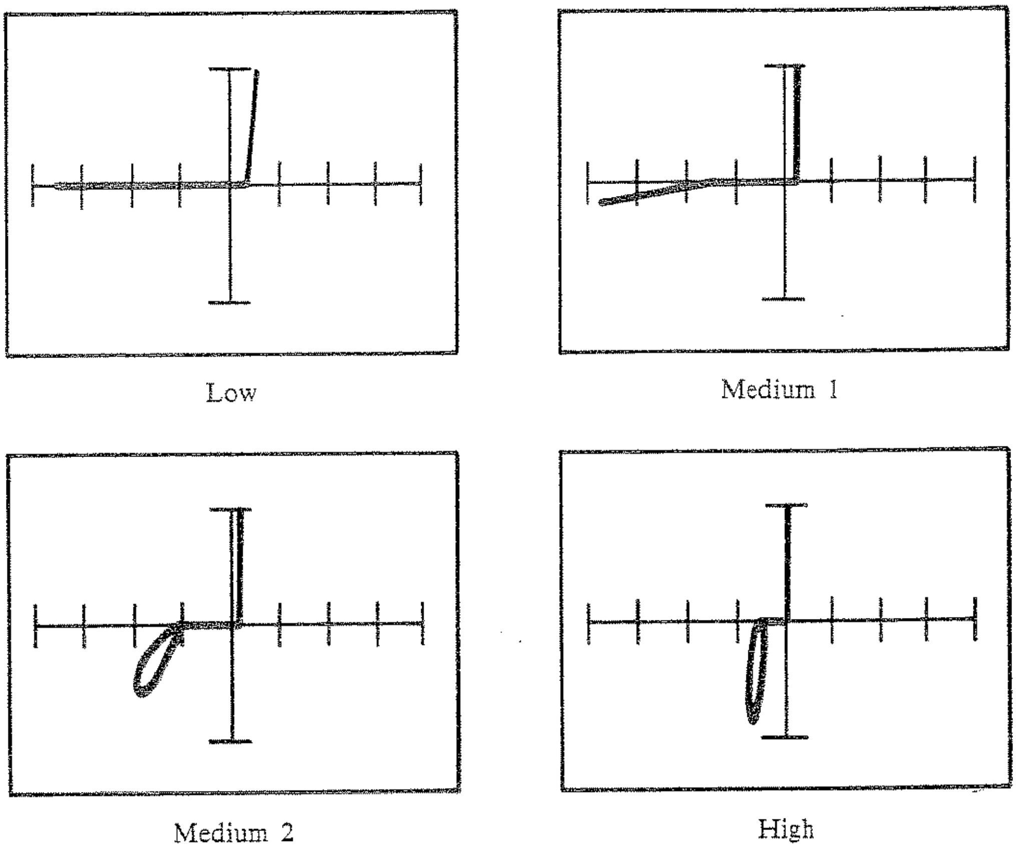


Figure 7-50. Signatures Between the V_{dd} Pin and V_{ss} Pin of a MC14011B at 60Hz

7.7 CMOS ANALOG SWITCH

CAUTION

WHEN TESTING CMOS COMPONENTS BE SURE TO FOLLOW ALL STATIC HANDLING PRECAUTIONS. THESE INCLUDE:

- Store and transport in conductive packaging.
- The person handling the device should be grounded with a one Megohm wrist strap.
- All surfaces should be conductive and connected to earth ground.
- All parts should be handled by their packages and not by the leads.

THESE ARE SOME OF THE MAJOR PRECAUTIONS — CHECK THE MANUFACTURER'S HANDLING TECHNIQUES FOR COMPLETE PROCEDURES.

NOTE: When testing CMOS devices, it is recommended that the V_{ss} and V_{dd} pins be shorted together to eliminate noise in the Tracker 2000 signatures.

NOTE: Tests were conducted in an independent laboratory to show that the Tracker test signals are safe to test CMOS, MOS and low power Schottky devices. Refer to the Appendixes at the back of this manual.

The MC14016B quad bilateral switch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each MC14016B consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator, and CMOS logic implementation.

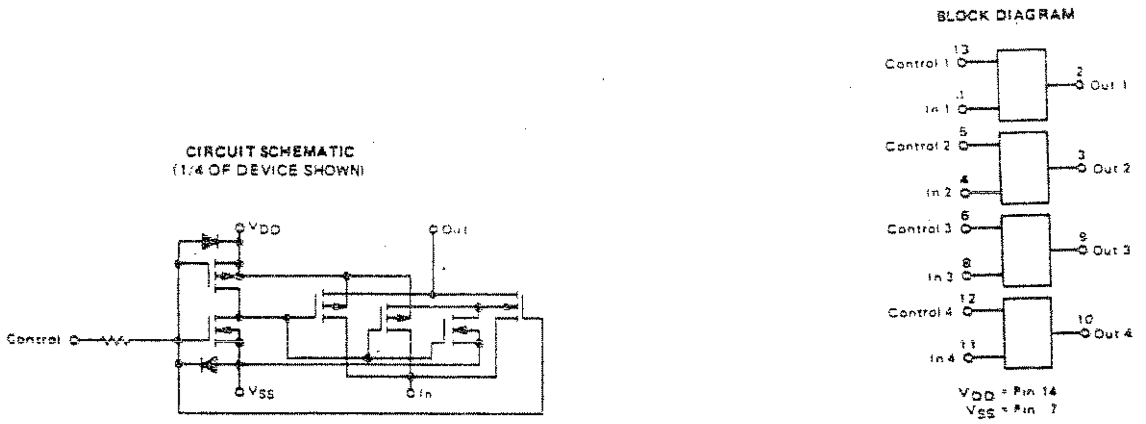
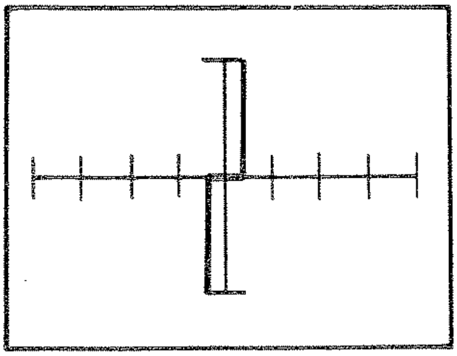
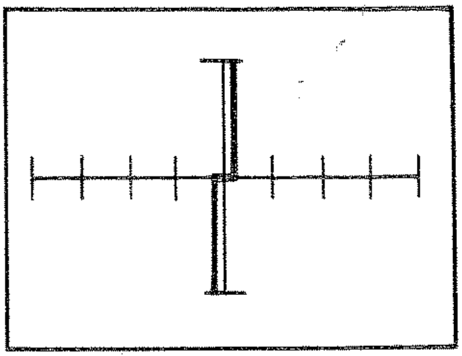


Figure 7-51. Pin Connections and Circuit Schematic of a MC14016B

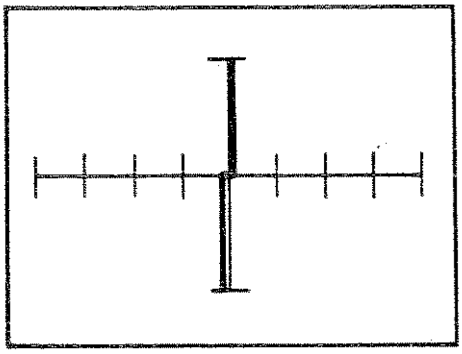
To test a 4016B analog switch we need to examine the input, output and control pins with respect to V_{ss}-V_{dd}. Figures 7-52 through 7-54 show the signatures of a good 4016B analog switch. Figure 7-55 exhibits the signatures of a defective 4016B. Comparing Figure 7-52 to Figure 7-55, the signatures show a significant difference between a good and defective device.



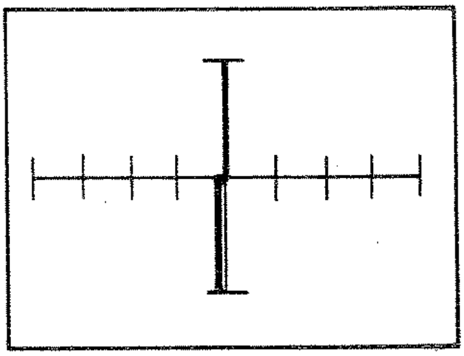
Low



Medium 1

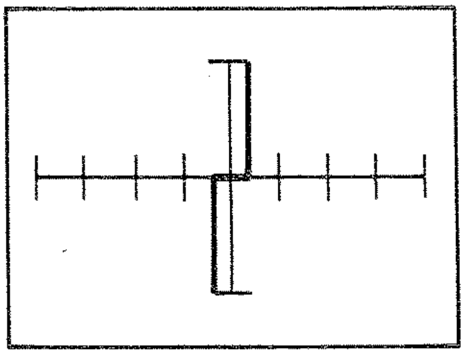


Medium 2

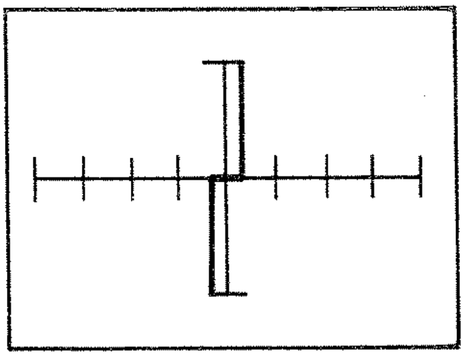


High

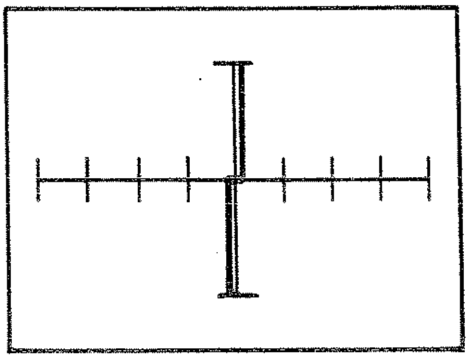
Figure 7-52. Signatures Between an Input Pin and V_{ss}-V_{dd} of an MC14016B Gate at 60Hz



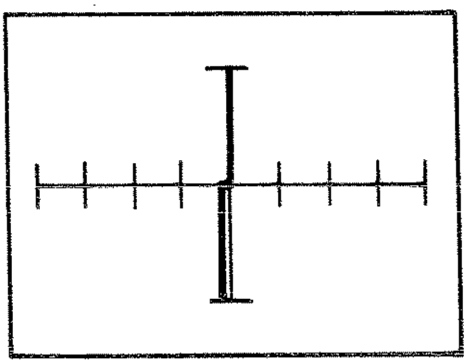
Low



Medium 1



Medium 2



High

Figure 7-53. Signatures Between an Output Pin and V_{ss}-V_{dd} of an MC14016B Gate at 60Hz

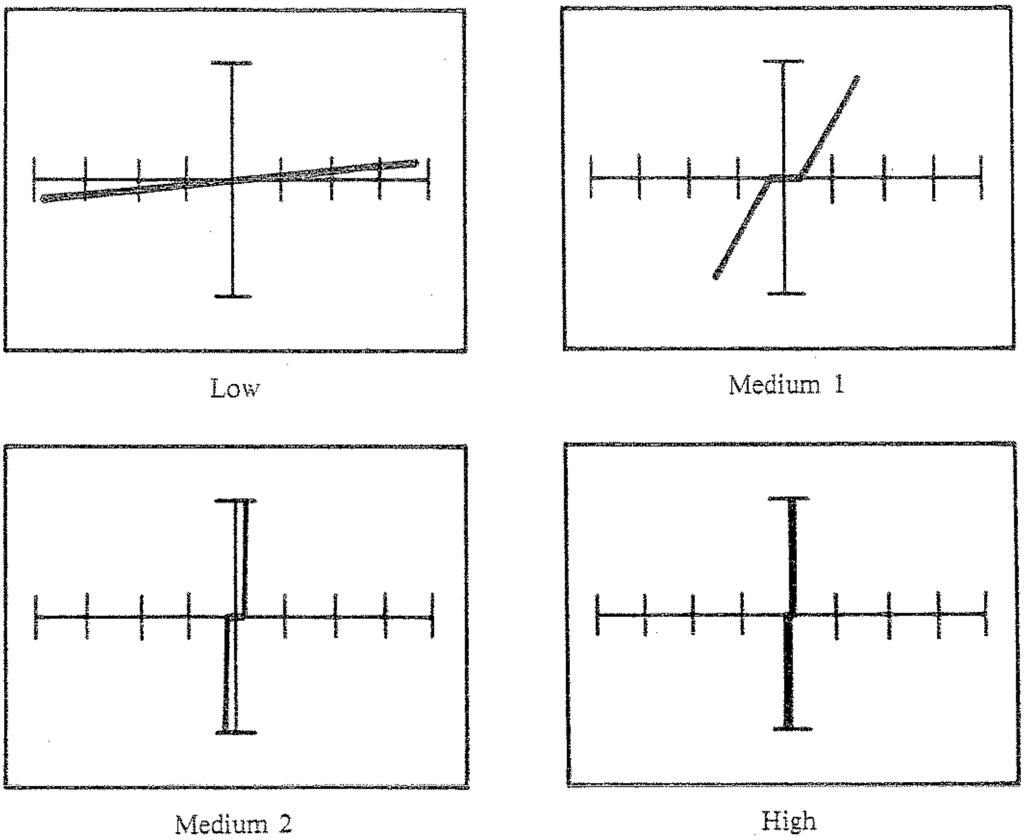


Figure 7-54. Signatures Between a Control Pin and V_{ss}-V_{dd} of an MC14016B Gate at 60Hz

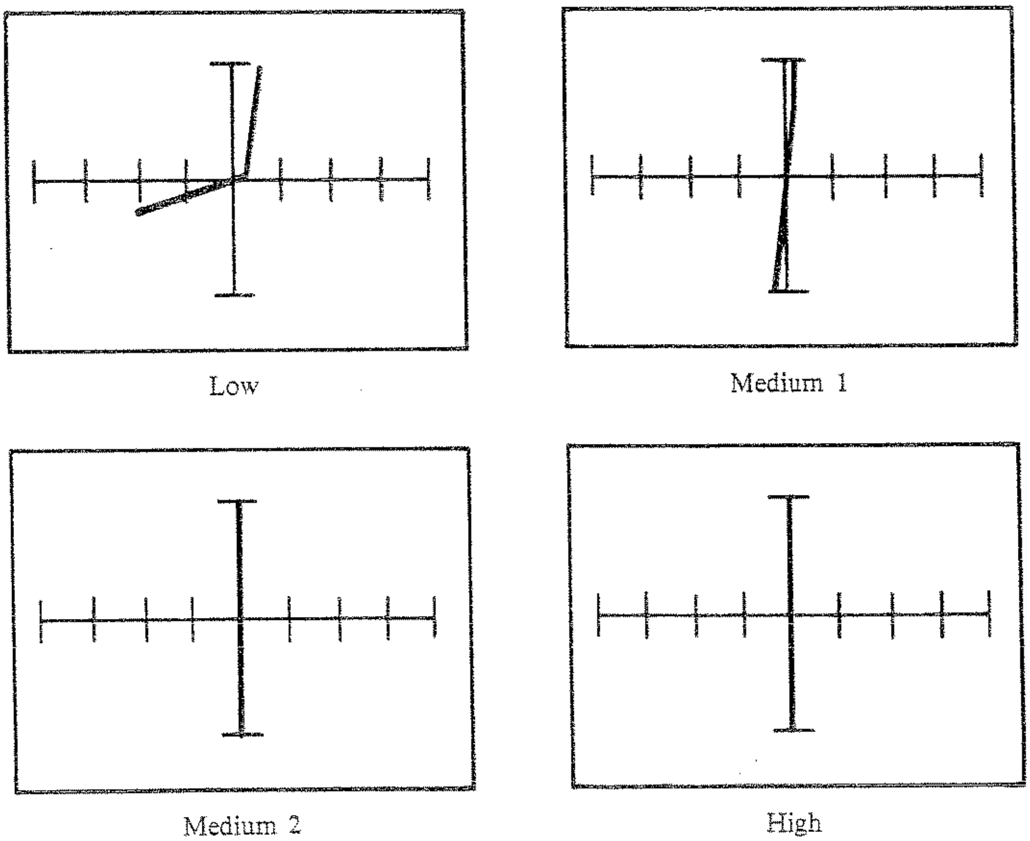
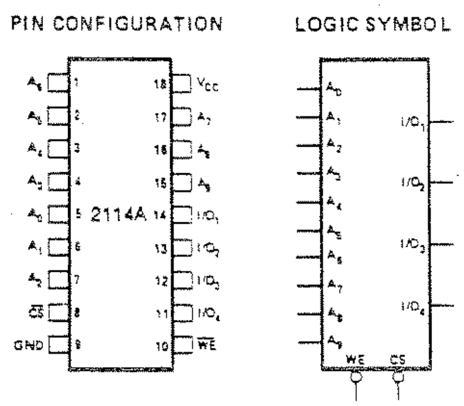
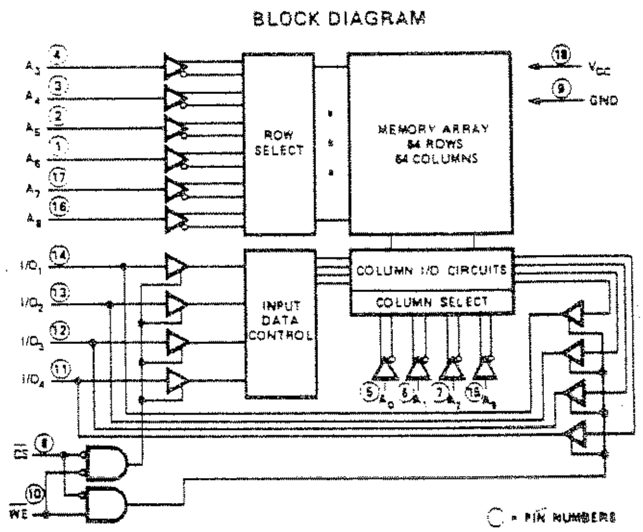


Figure 7-55. Signatures Between an Input Pin and V_{ss}-V_{dd} of a Defective 4016B at 60Hz

7.8 MOS STATIC RAM

The 2114A is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using HMOS, a high performance MOS technology. It uses fully DC stable (static) circuitry throughout, both in array and decoding.





PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O_1–I/O_4	DATA INPUT/OUTPUT	

Figure 7-56. Schematics and Pin Configuration of a Static RAM 2114A.

Figures 7-57 through 7-61 show the signatures of the Address, CS, WE, I/O, and V_{CC} pins with respect to the ground pin. Signatures of the Address, CS and WE are similar because they have similar fabrication structure.

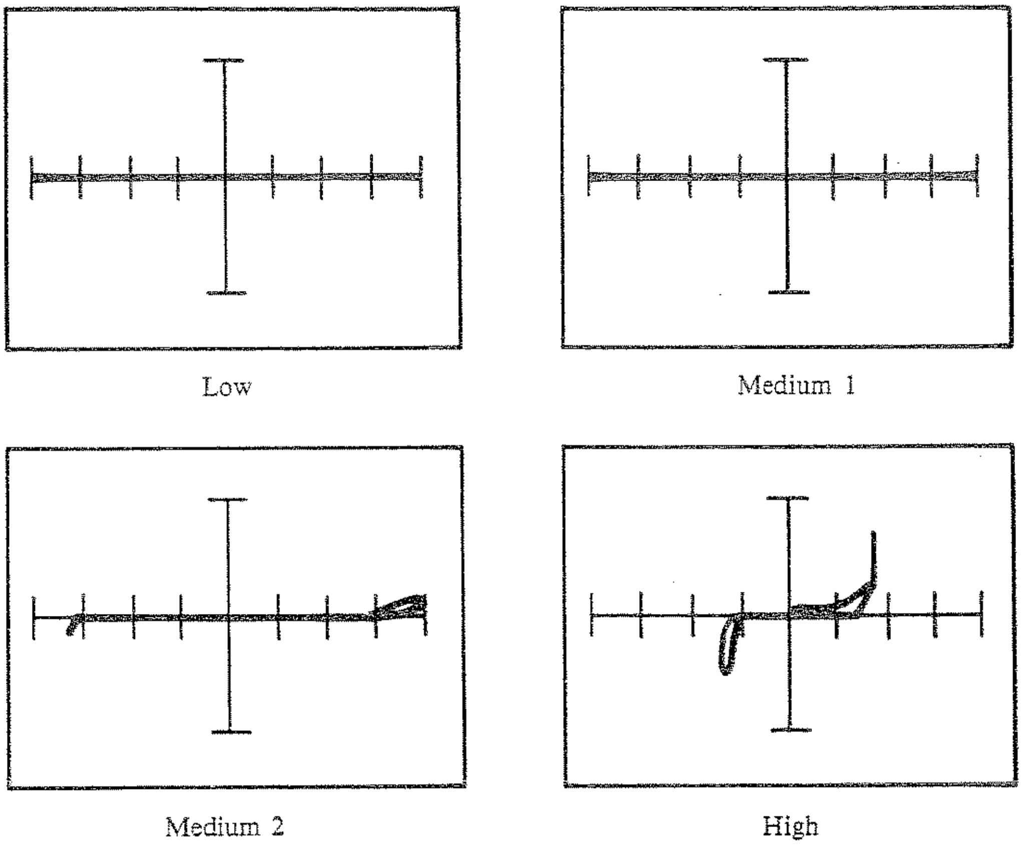


Figure 7-57. Signatures Between an Address Pin and the Ground Pin of a 2114A Static RAM at 60Hz

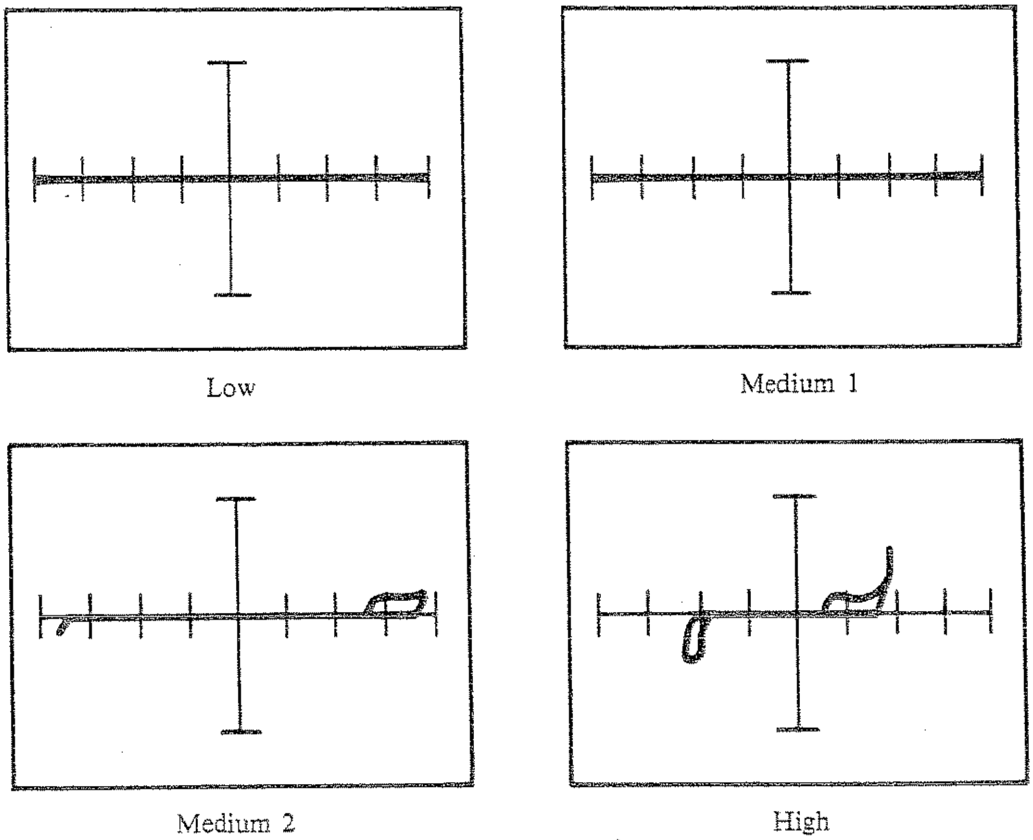


Figure 7-58. Signatures Between the CS Pin and the Ground Pin of a 2114A Static RAM at 60Hz

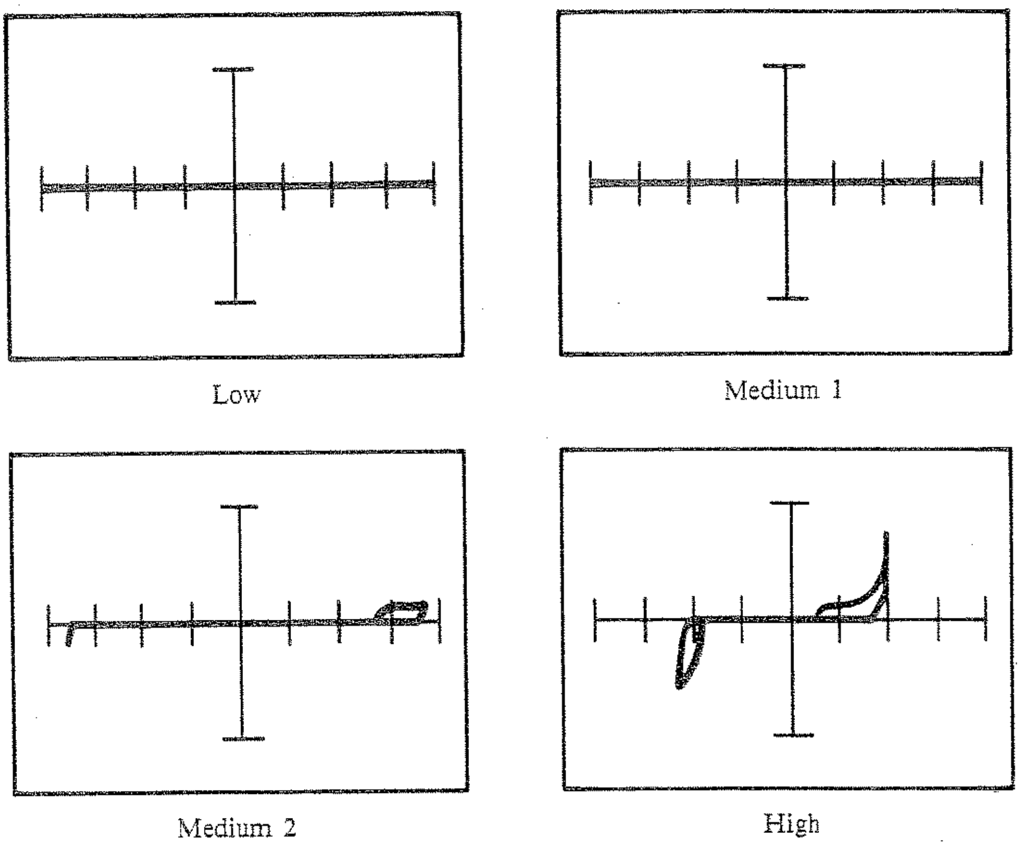


Figure 7-59. Signatures Between the WE Pin and the Ground Pin of a 2114A Static RAM at 60Hz

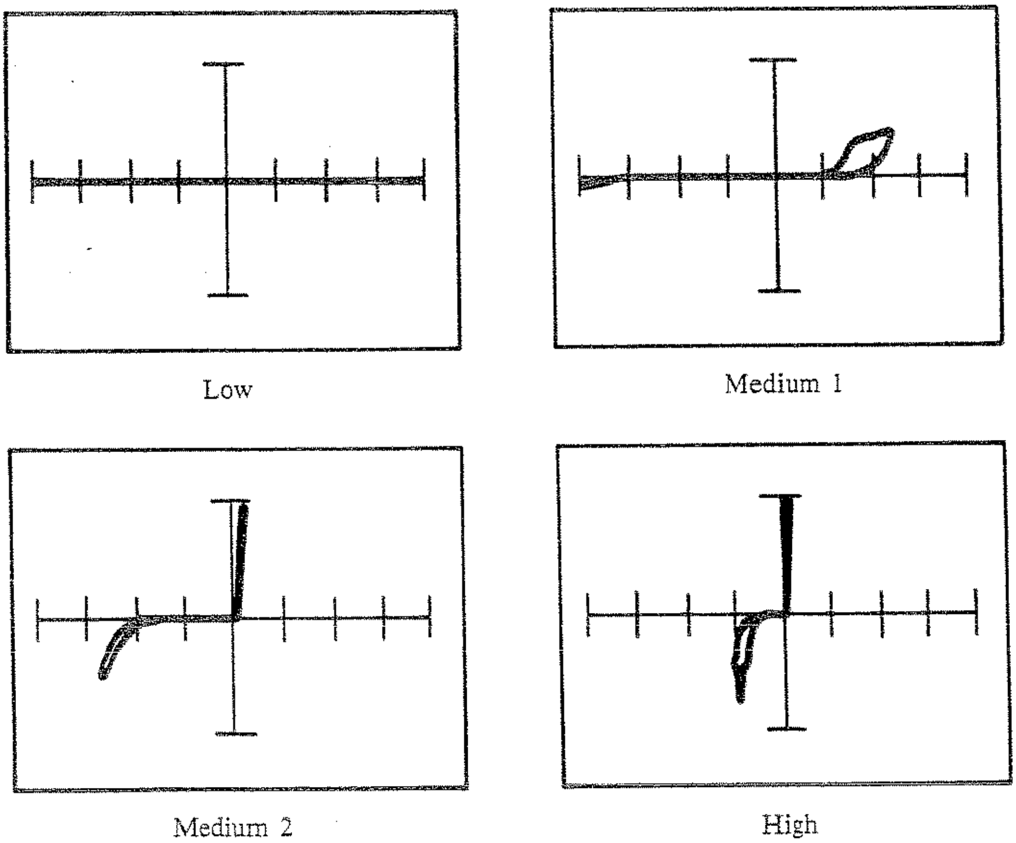


Figure 7-60. Signatures Between the I/O Pin and the Ground Pin of a 2114A Static RAM at 60Hz

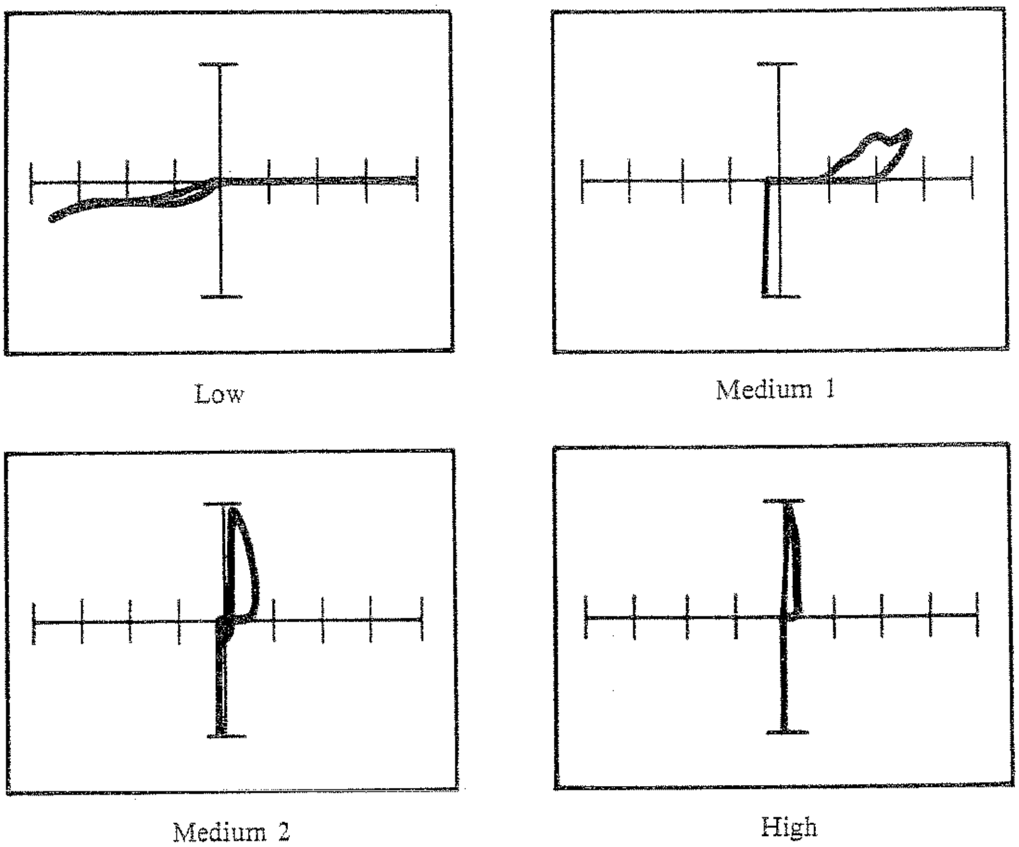


Figure 7-61. Signatures Between the V_{CC} Pin and the Ground Pin of a 2114A Static RAM at 60Hz

7.9 EPROM

The 2708JL is an ultraviolet light erasable, electrically programmable, read only memory. The 2708JL has 8,192 bits organized as 1024 words of 8-bit length. These devices are fabricated using N-channel silicon gate technology for high speed and simple interface with MOS and bipolar circuits. The data outputs for all three circuits are tri-state for connecting multiple devices on a common bus. The pin configuration of a 2708JL is shown in Figure 7-62. The signatures of various pins with respect to V_{SS} are shown in Figures 7-63 through 7-69. Signatures may vary from manufacturer to manufacturer; however, in general, the signatures are similar.

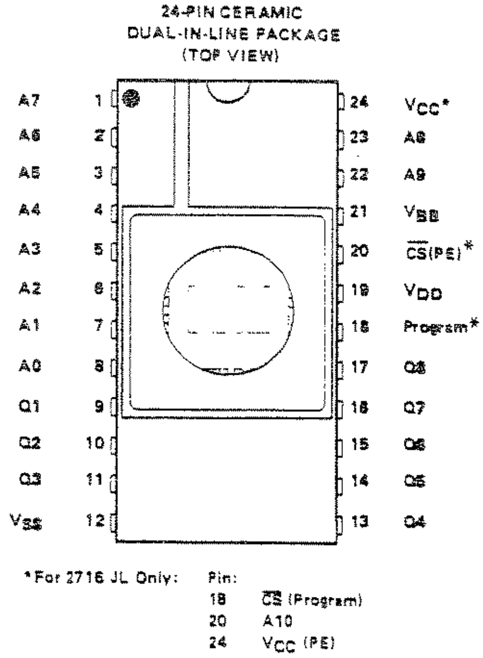


Figure 7-62. Pin Configuration of a 2708JL

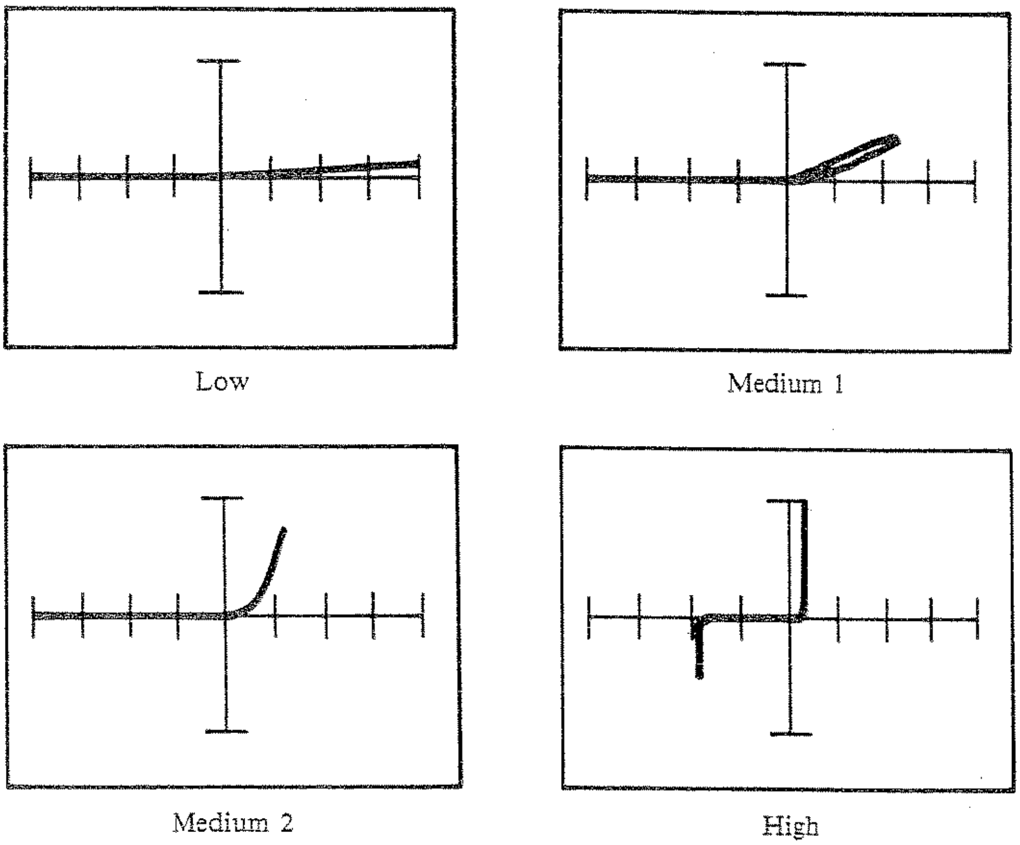


Figure 7-63. Signatures Between an Address Pin and the V_{SS} Pin of a 2708JL at 60Hz

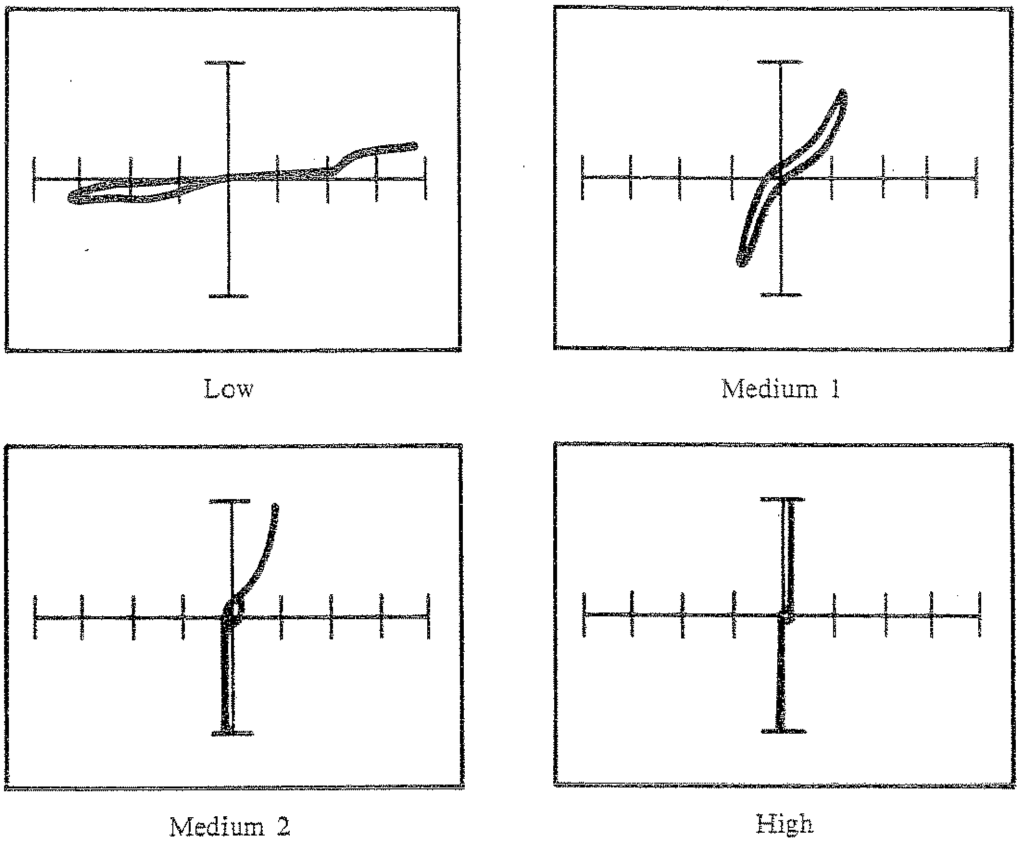


Figure 7-64. Signatures Between an Output Pin and the V_{SS} Pin of a 2708JL at 60Hz

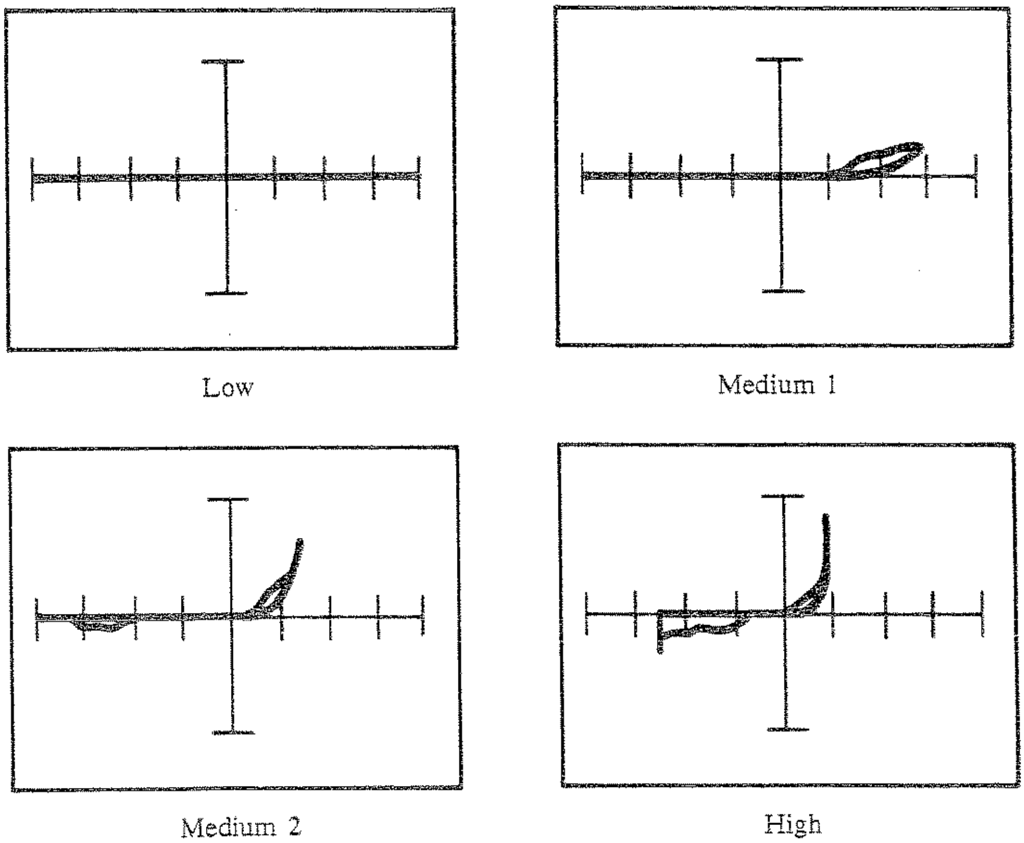


Figure 7-65. Signatures Between the Program Pin (18) and V_{SS} Pin of a 2708JL at 60Hz

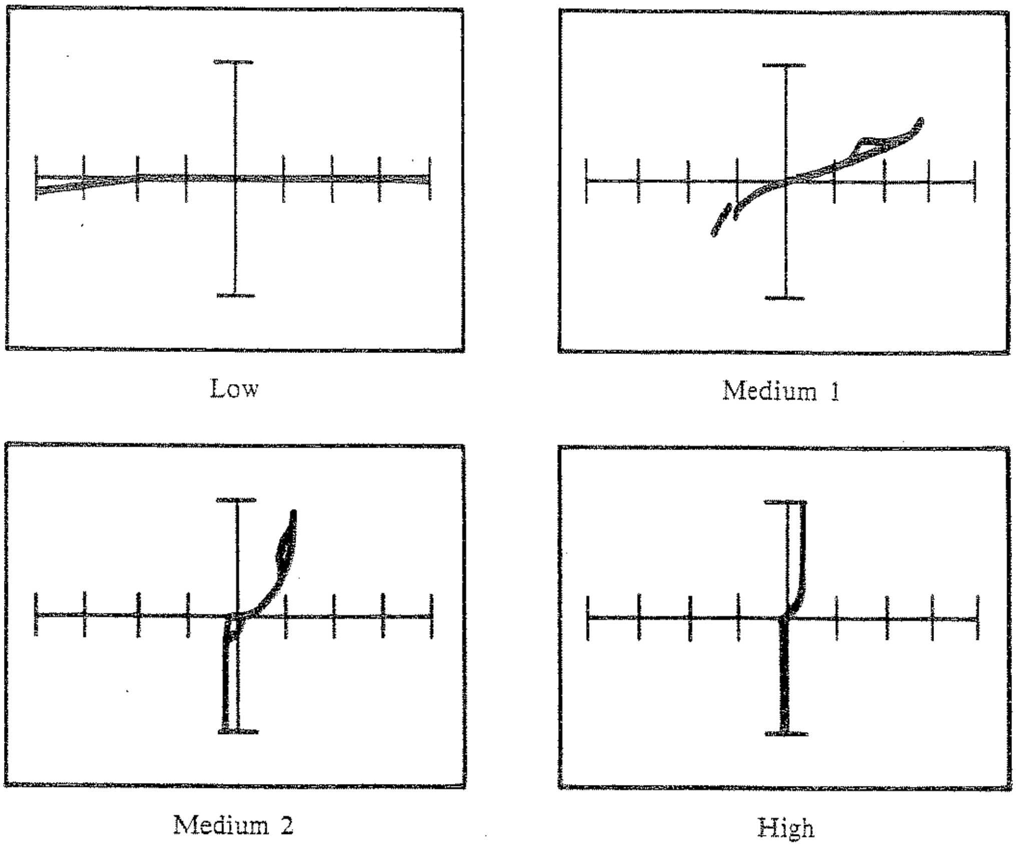


Figure 7-66. Signatures Between the V_{dd} Pin (19) and the V_{ss} Pin of a 2708JL at 60Hz

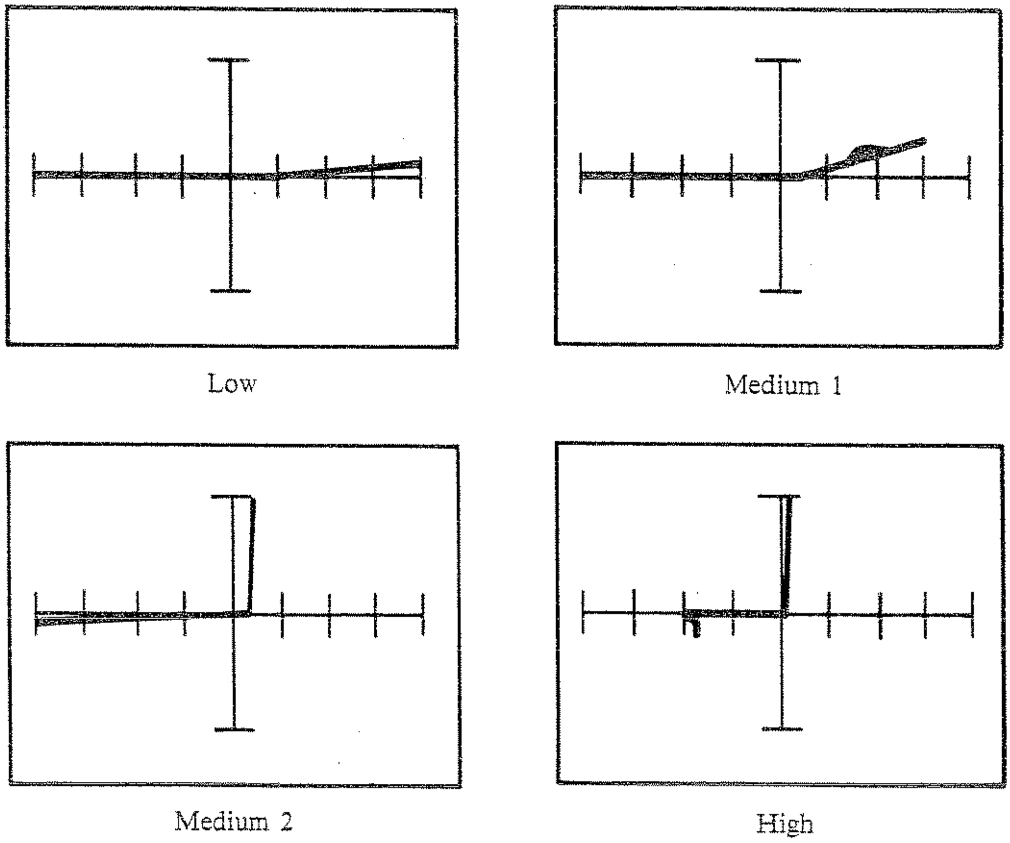
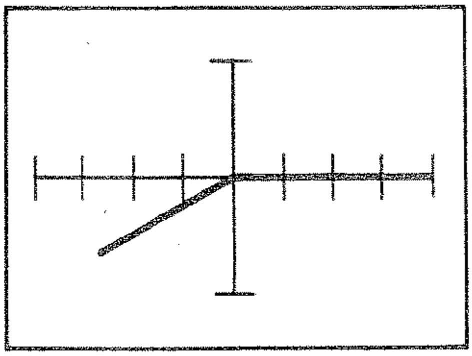
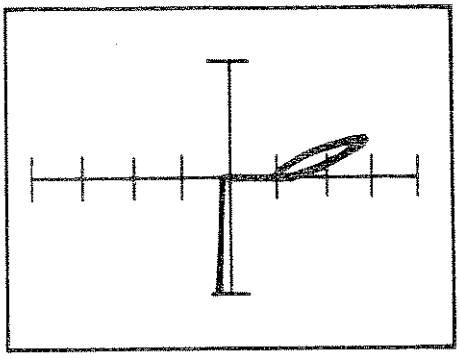


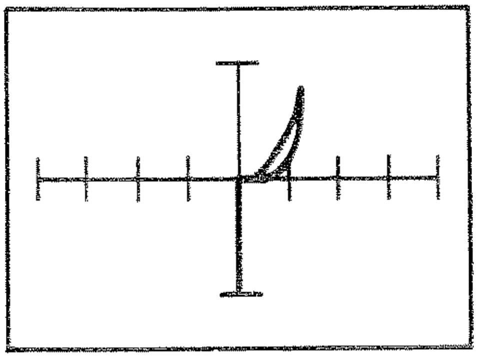
Figure 7-67. Signatures Between the CS Pin (20) and the V_{ss} Pin of a 2708JL at 60Hz



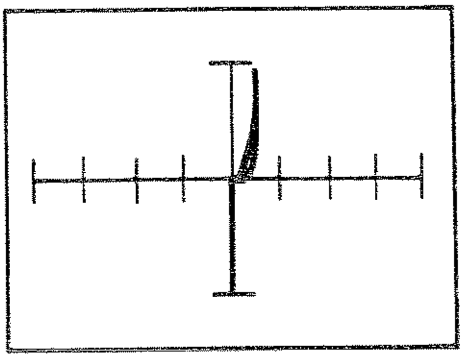
Low



Medium 1

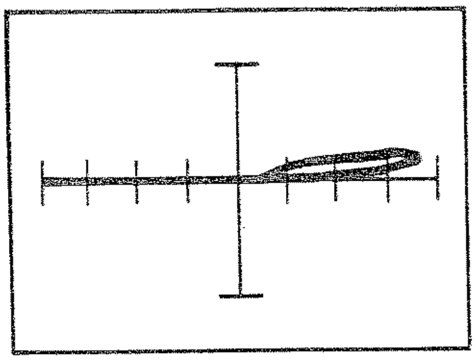


Medium 2

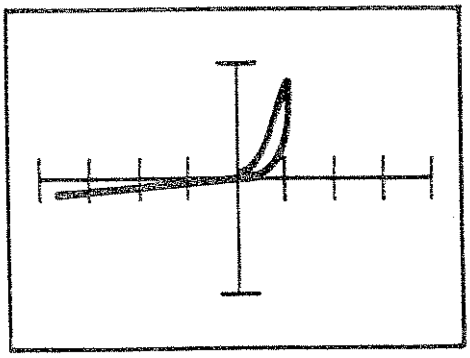


High

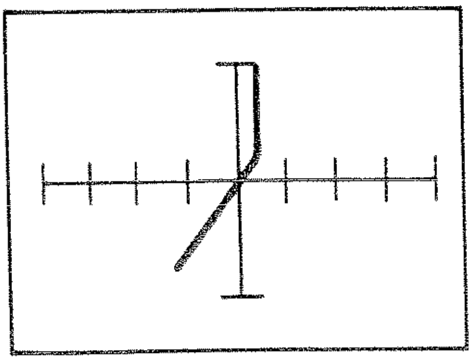
Figure 7-68. Signatures Between the V_{bb} Pin (21) and the V_{ss} Pin of a 2708JL at 60Hz



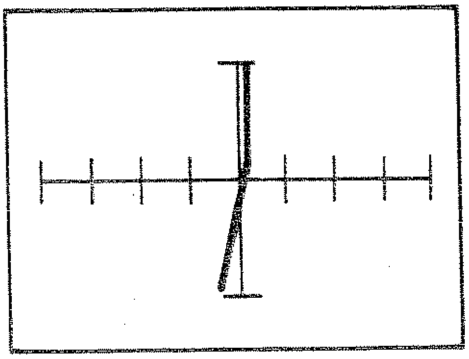
Low



Medium 1



Medium 2



High

Figure 7-69. Signatures Between the V_{cc} Pin (24) and the V_{ss} Pin of a 2708JL at 60Hz

7.10 BIPOLAR PROM

The Monolithic Memories 6301-1J is a 256x4 prom with tri-state outputs. It is implemented with standard schottky technology. The pin configuration of a 6301-1J is shown in Figure 7-70. The signatures of various pins with respect to ground are shown in Figures 7-71 through 7-74.

Pin Configurations

53/6300-1
53/6301-1

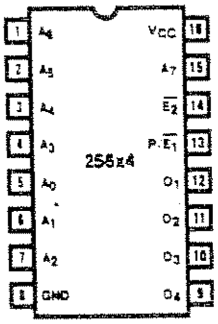
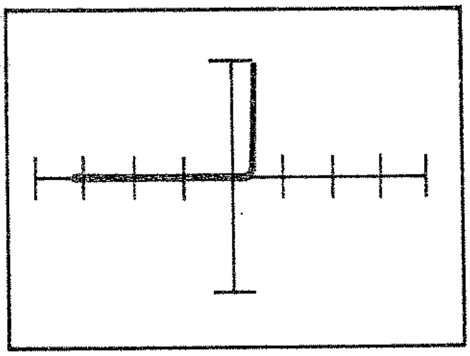
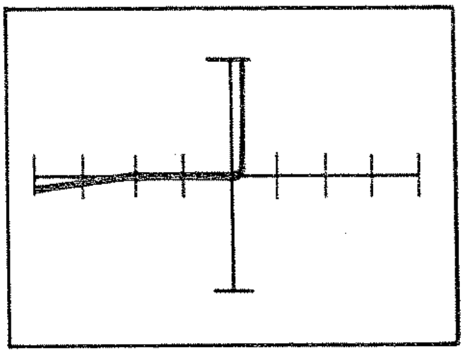


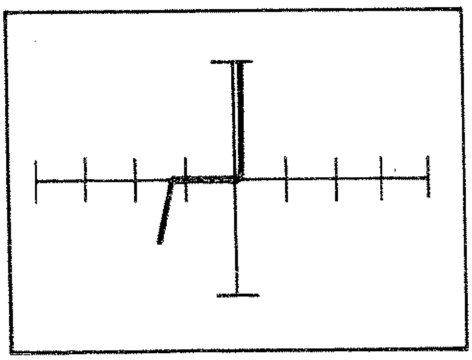
Figure 7-70. Pin Configuration of a 6301-1J



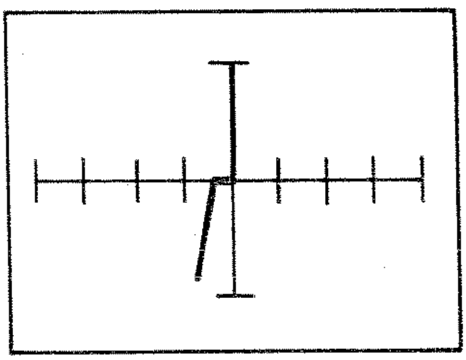
Low



Medium 1



Medium 2



High

Figure 7-71. Signatures Between an Address Pin and the Ground Pin of a 6301-1J at 60Hz

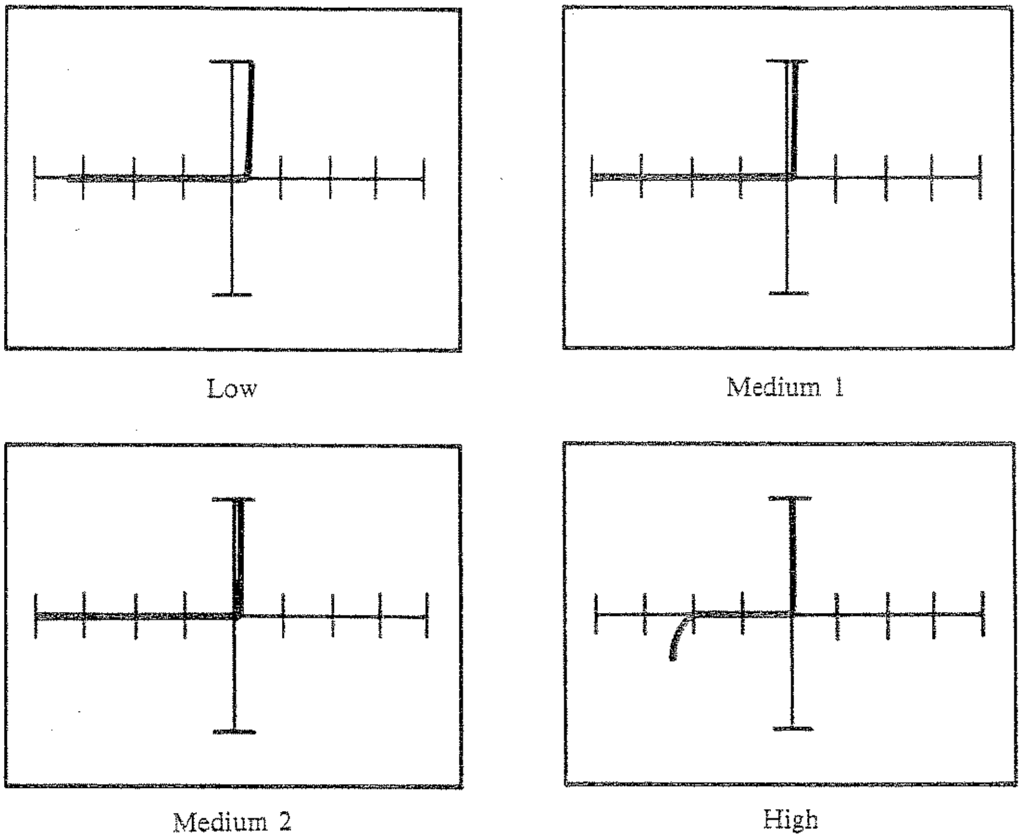


Figure 7-72. Signatures Between an Output Pin and the Ground Pin of a 6301-1J at 60Hz

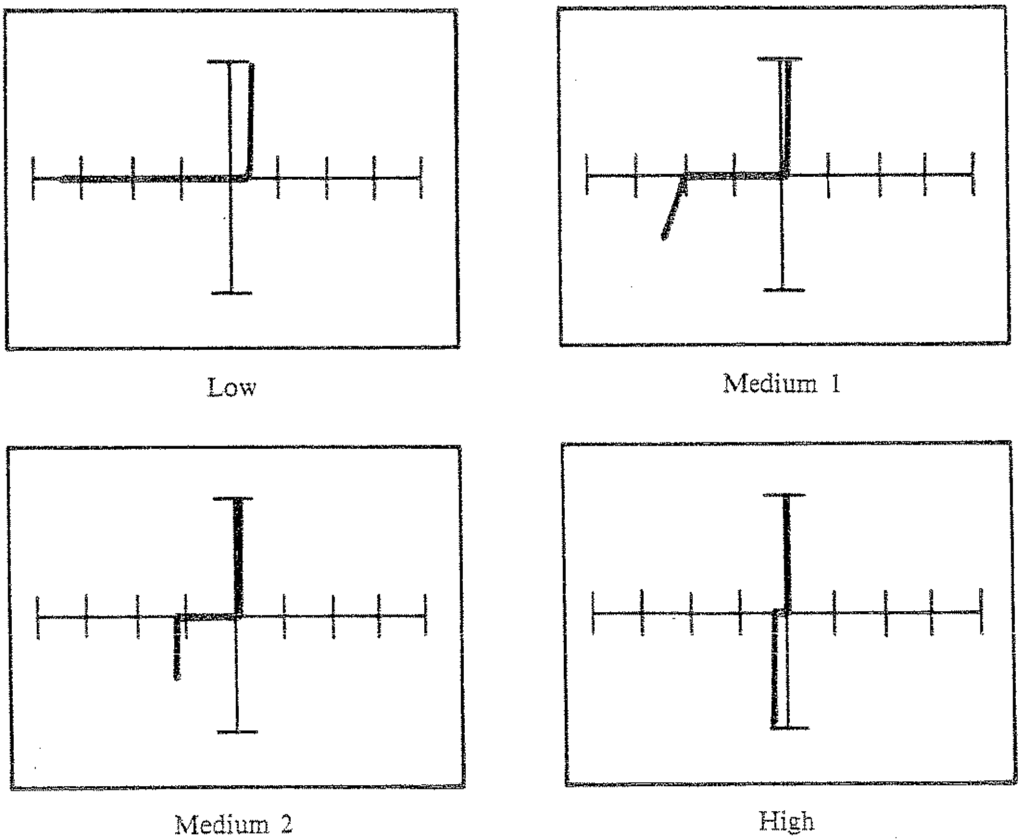


Figure 7-73. Signatures Between the Enable Pin (E_2) and the Ground Pin of a 6301-1J at 60Hz

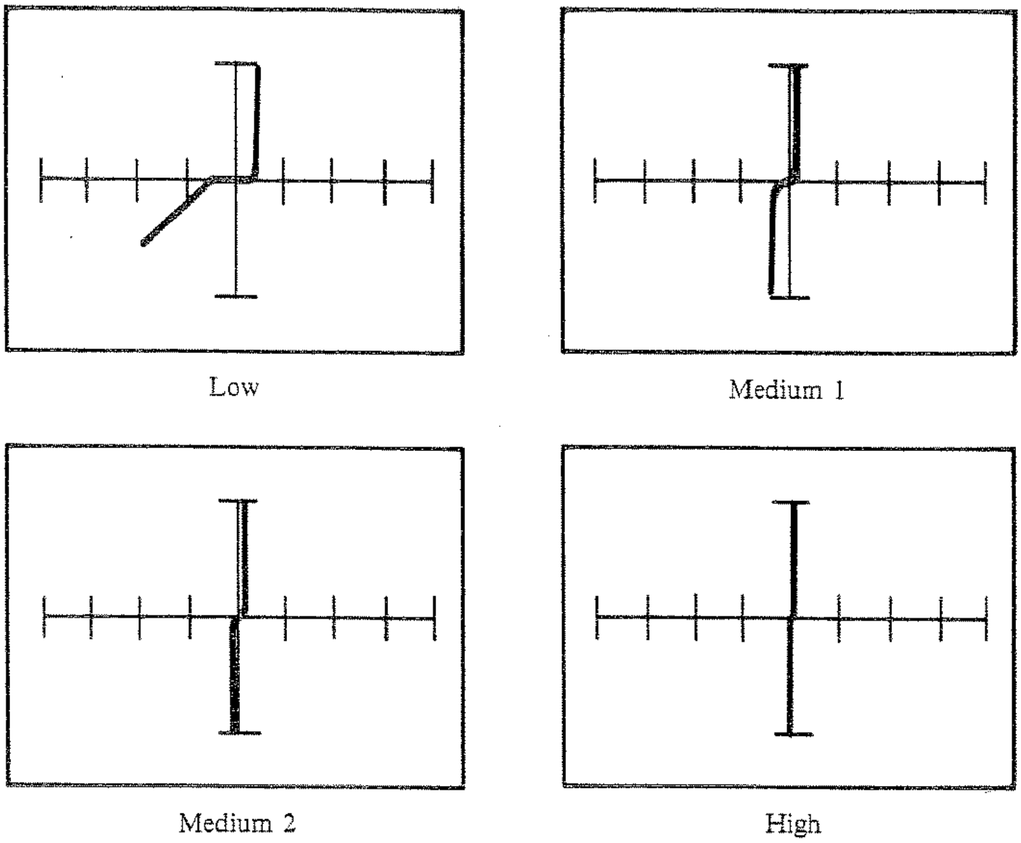


Figure 7-74. Signatures Between the V_{cc} Pin and the Ground Pin of a 6301-1J at 60Hz

7.11 DIGITAL TO ANALOG CONVERTER

The National DAC0800L is a monolithic, 8-bit, high speed, current output, digital to analog converter implemented with bipolar technology. Figure 7-75 shows the pin configuration and equivalent circuit of a DAC0800L. The signatures of various pins with respect to V− are shown in Figures 7-76 through 7-82.

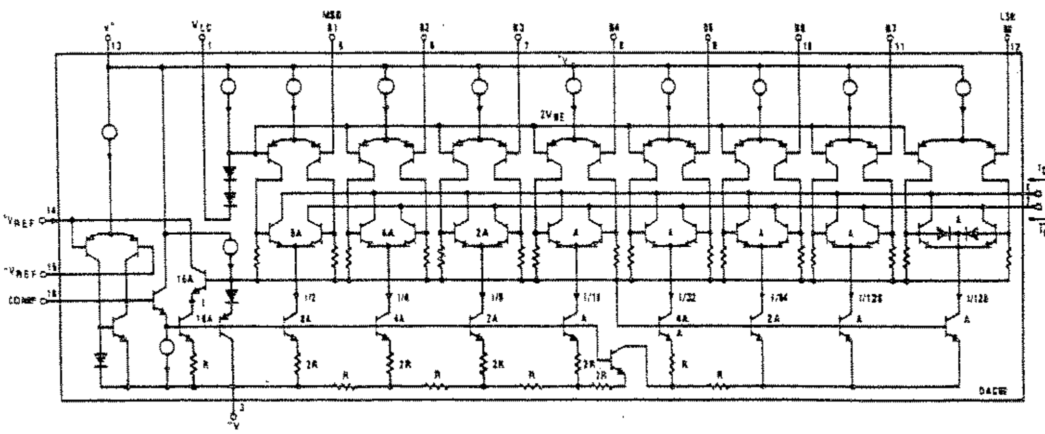


Figure 7-75. Pin Configuration and Equivalent Circuit of a DACO800L

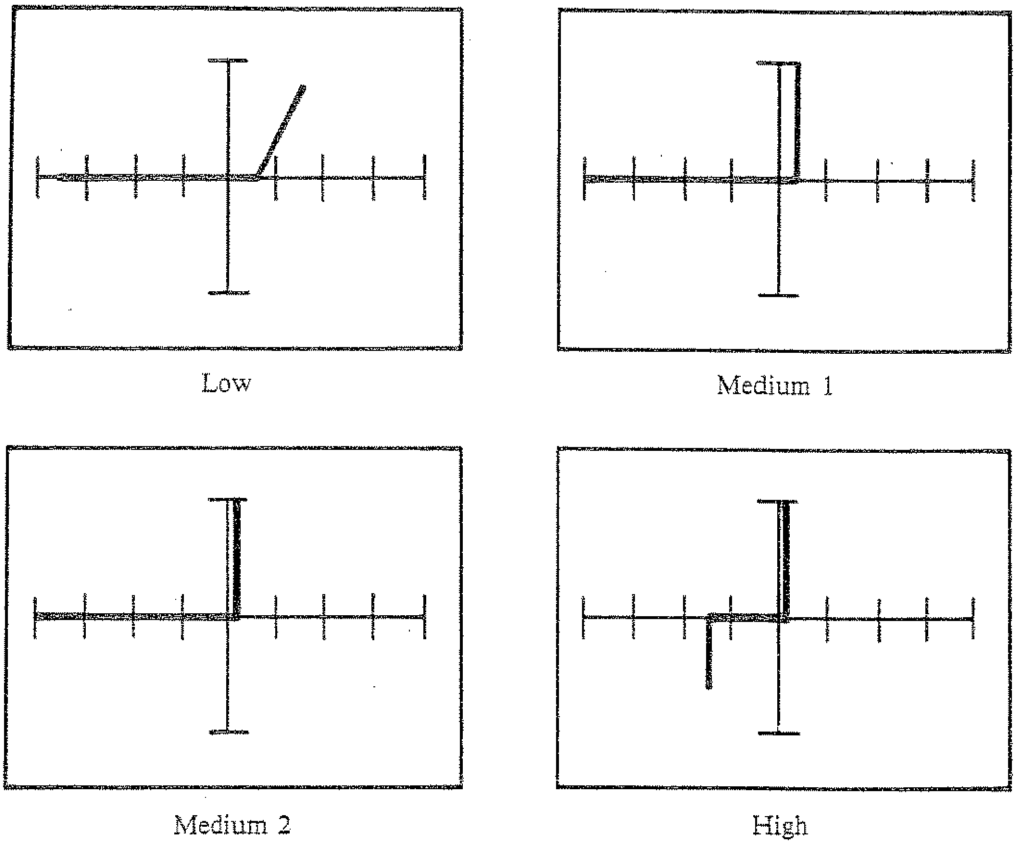


Figure 7-76. Signatures Between the Threshold Pin (V_{lc}) and the V− Pin of a DAC0800L at 60Hz

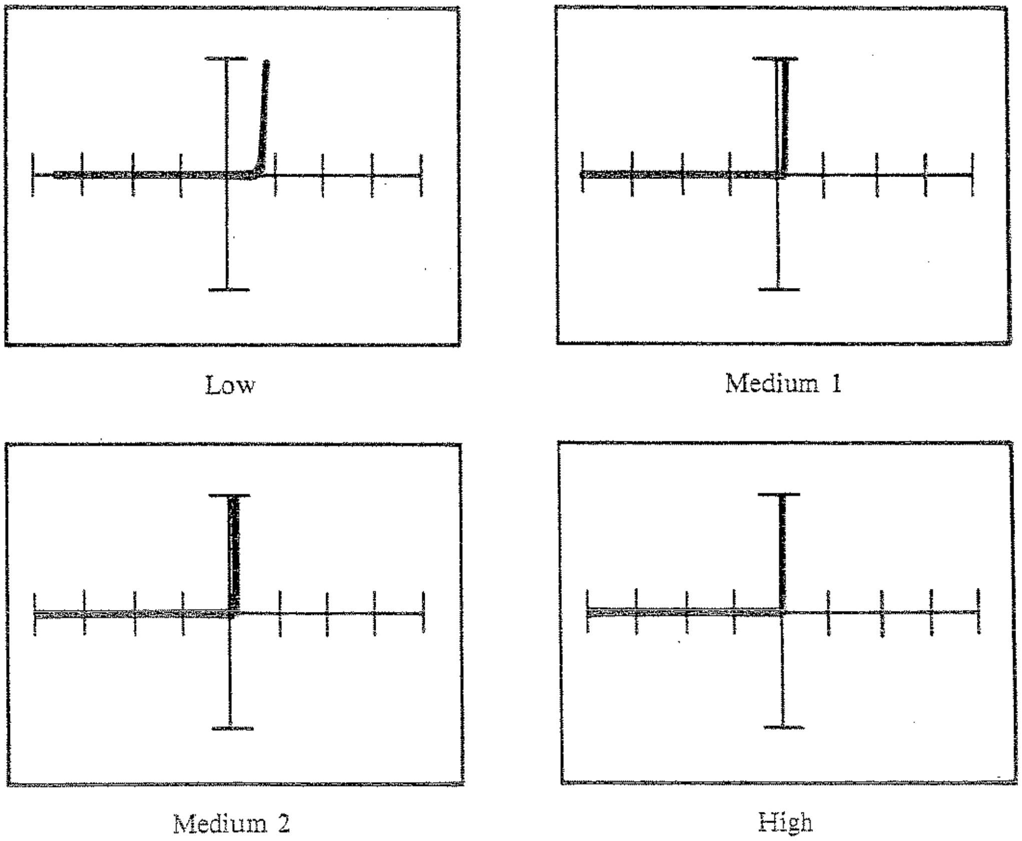
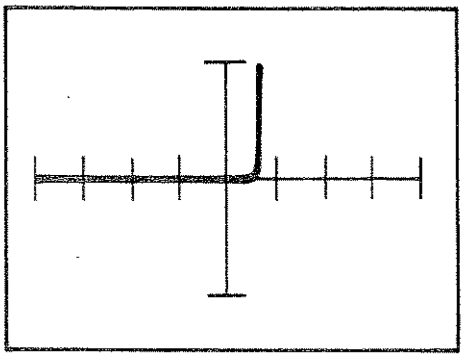
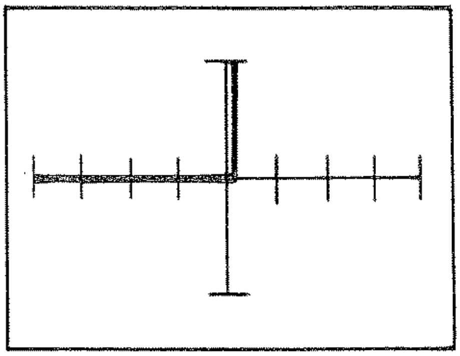


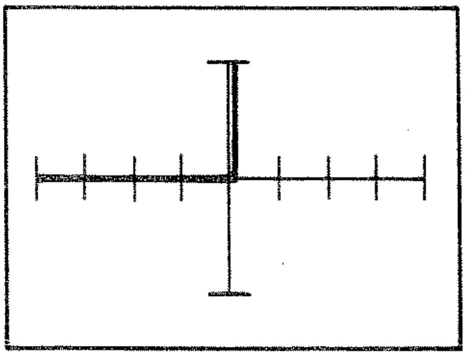
Figure 7-77. Signatures Between the I_{out} Pin (4) and the V− Pin of a DAC0800L at 60Hz



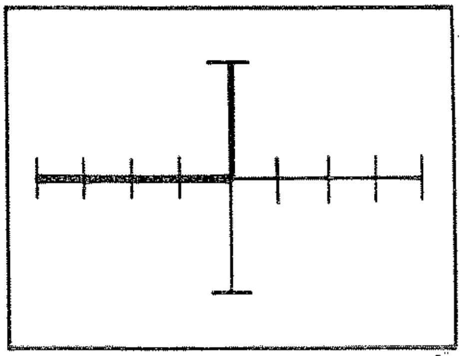
Low



Medium 1

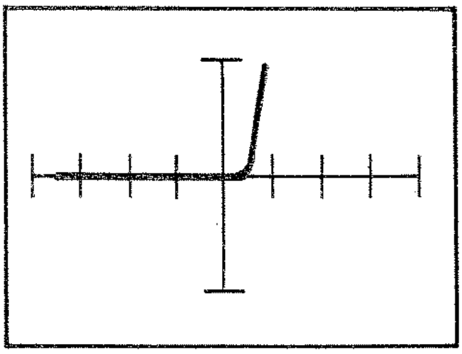


Medium 2

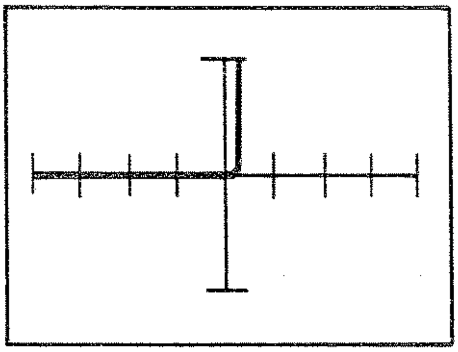


High

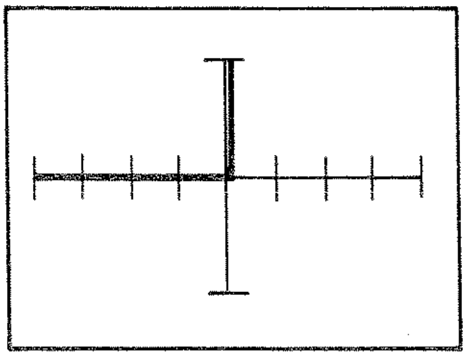
Figure 7-78. Signatures Between a Digital Input Pin and the V− Pin of a DAC0800L at 60Hz



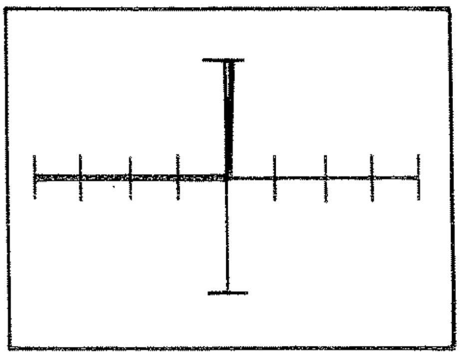
Low



Medium 1



Medium 2



High

Figure 7-79. Signatures Between the Reference Pin $V_{ref(+)}$ and the V− Pin of a DAC0800L at 60Hz

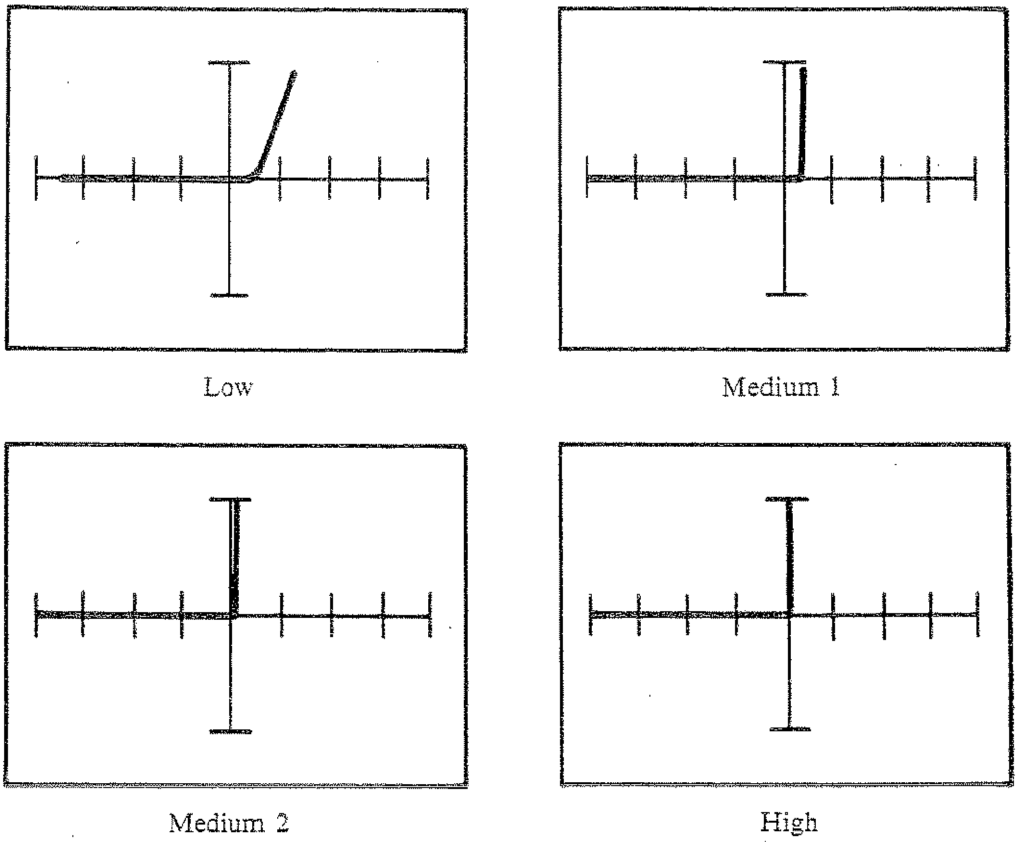


Figure 7-80. Signatures Between the Reference $V_{ref(-)}$ Pin and the V− Pin of a DAC0800L at 60Hz

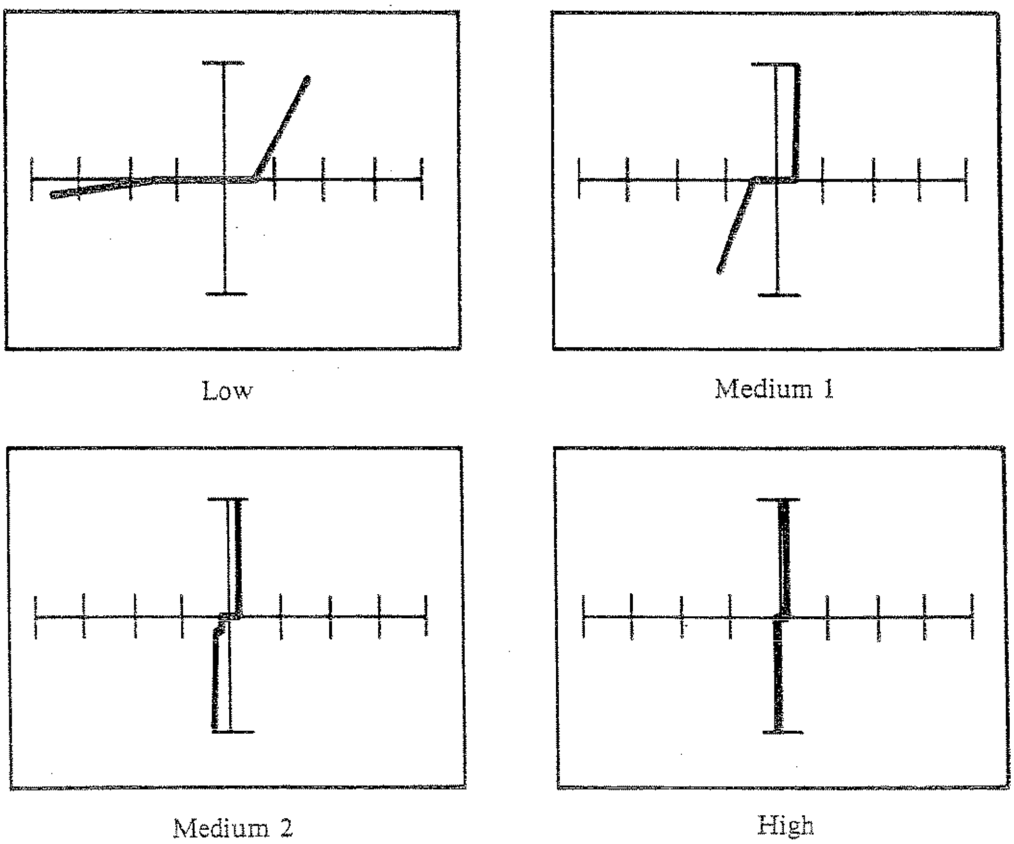


Figure 7-81. Signatures Between the Compensation Pin and the V− Pin of a DAC0800L at 60Hz

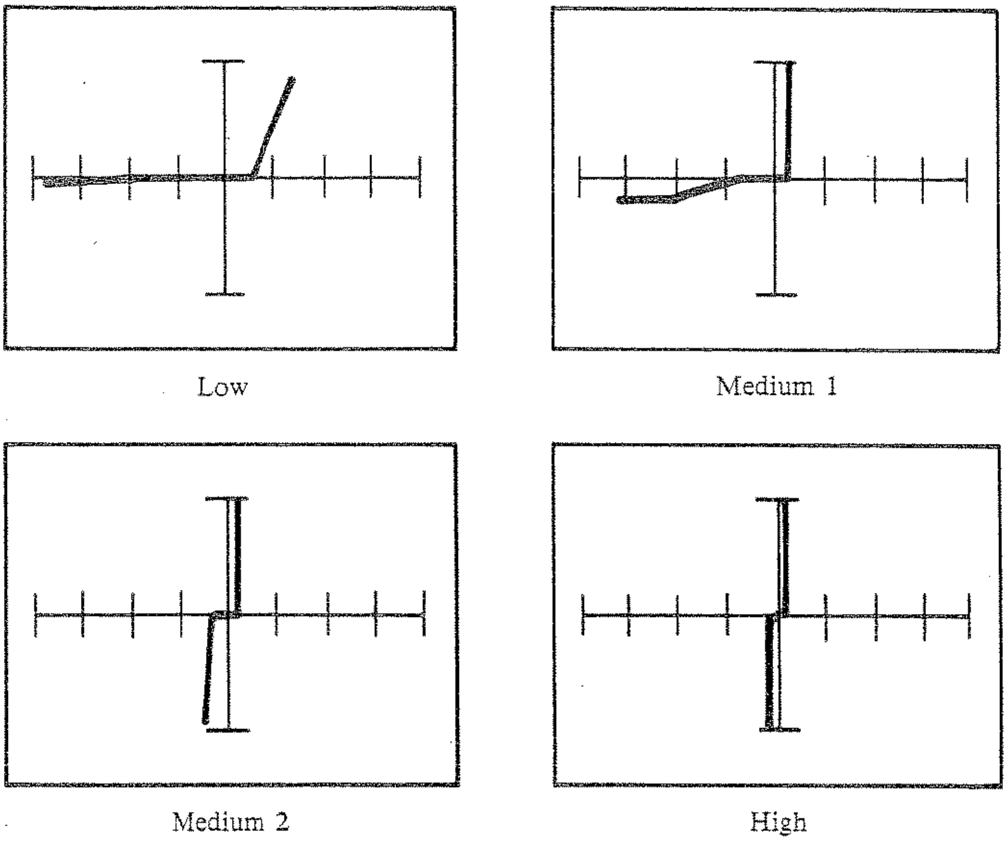


Figure 7-82. Signatures Between the V+ and V− Pins of a DAC0800L at 60Hz

7.12 MICROPROCESSORS

The 8080A is an 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using an N-channel silicon gate MOS process. Figure 7-83 shows the pin configuration of an 8080A microprocessor.

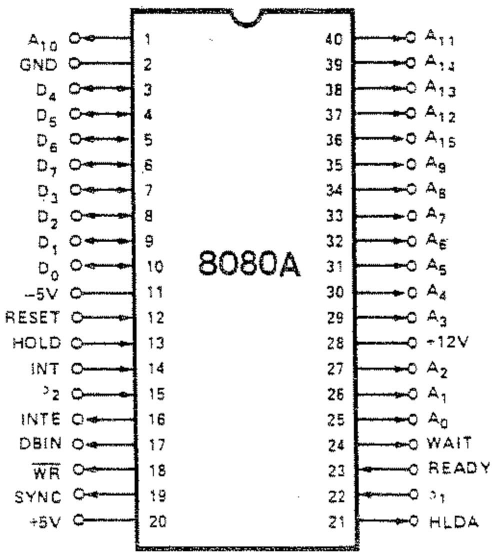


Figure 7-83. Pin Configuration of an 8080A

The signatures of various pins with respect to the −5V pin are shown in Figures 7-84 through 7-89.

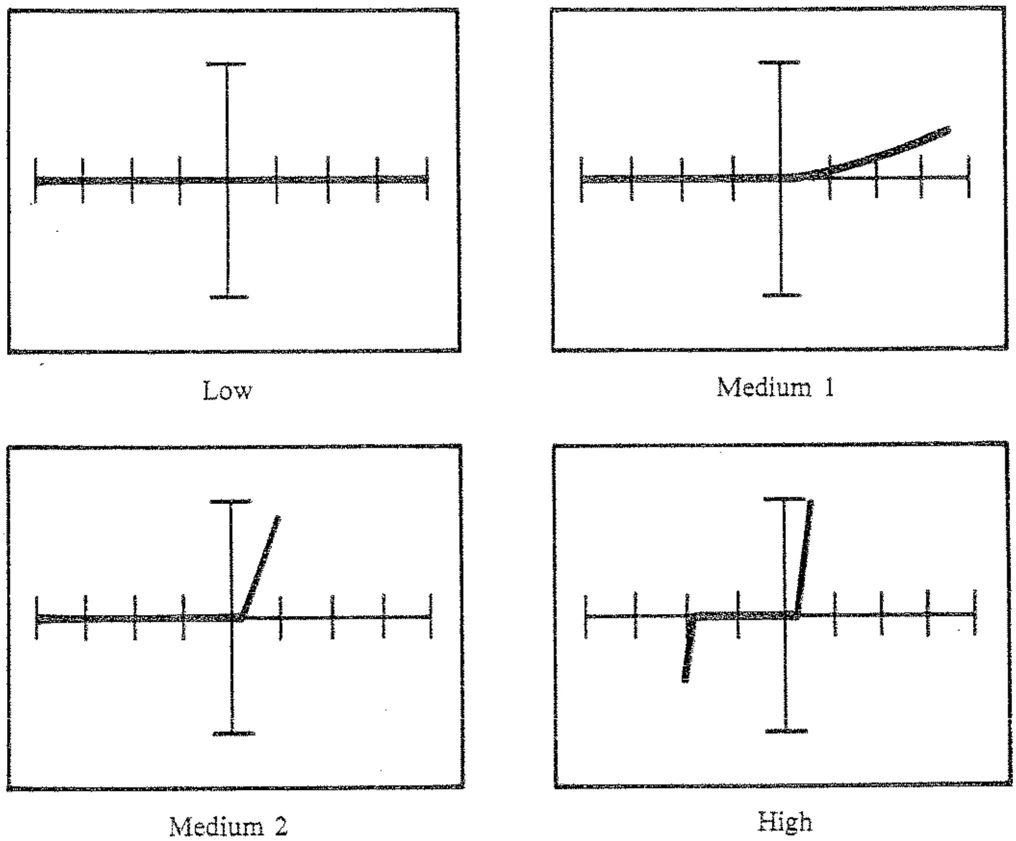


Figure 7-84. Signatures Between an Address Pin and the −5V Pin of an 8080A at 60Hz

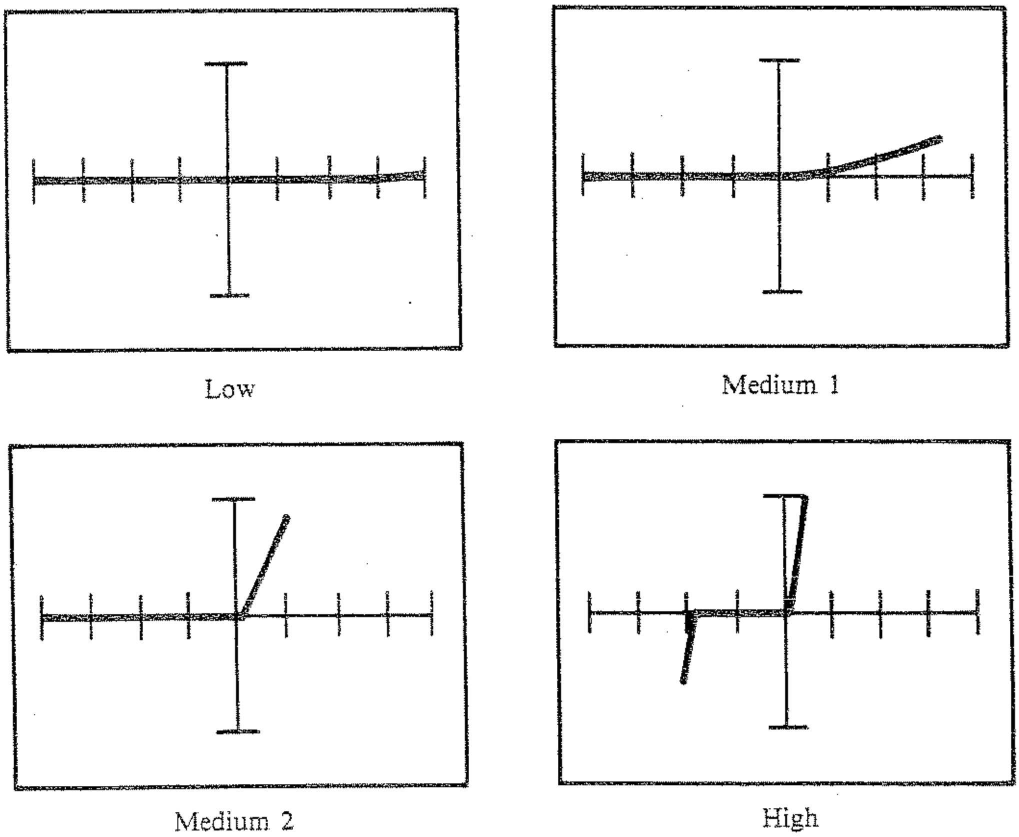


Figure 7-85. Signatures Between a Data Pin and the −5V Pin of an 8080A at 60Hz

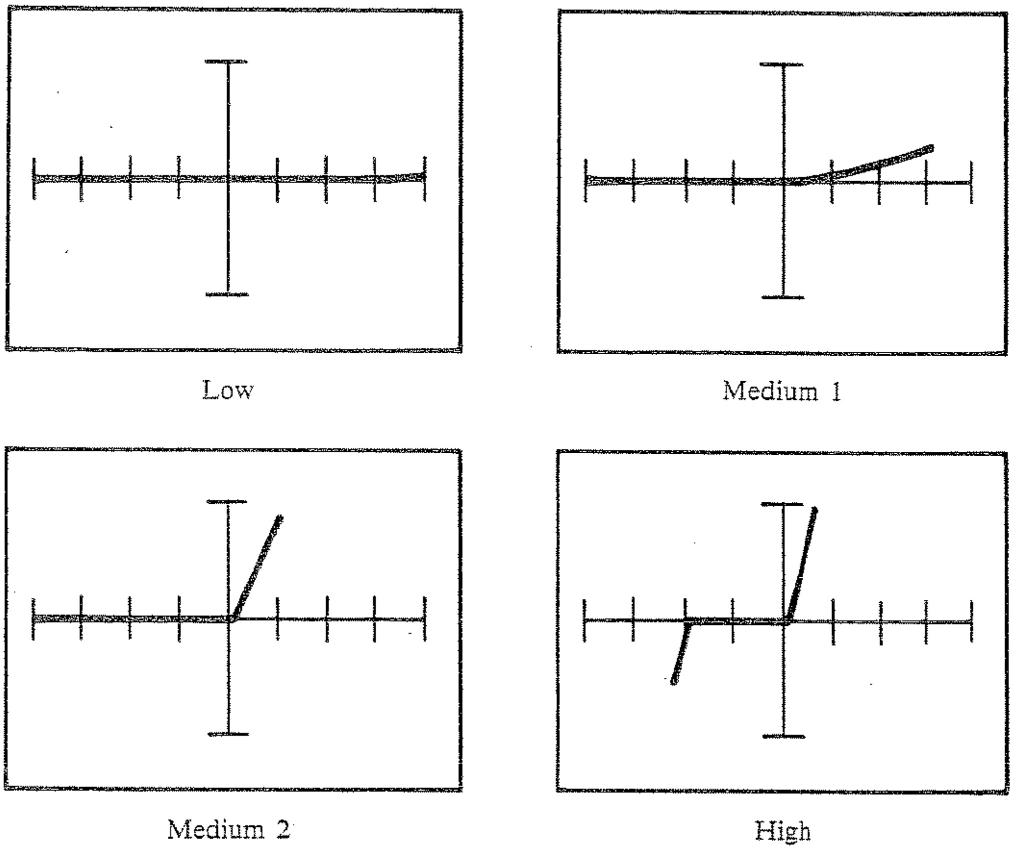


Figure 7-86. Signatures Between the Reset Pin (12) and the −5V Pin of an 8080A at 60Hz

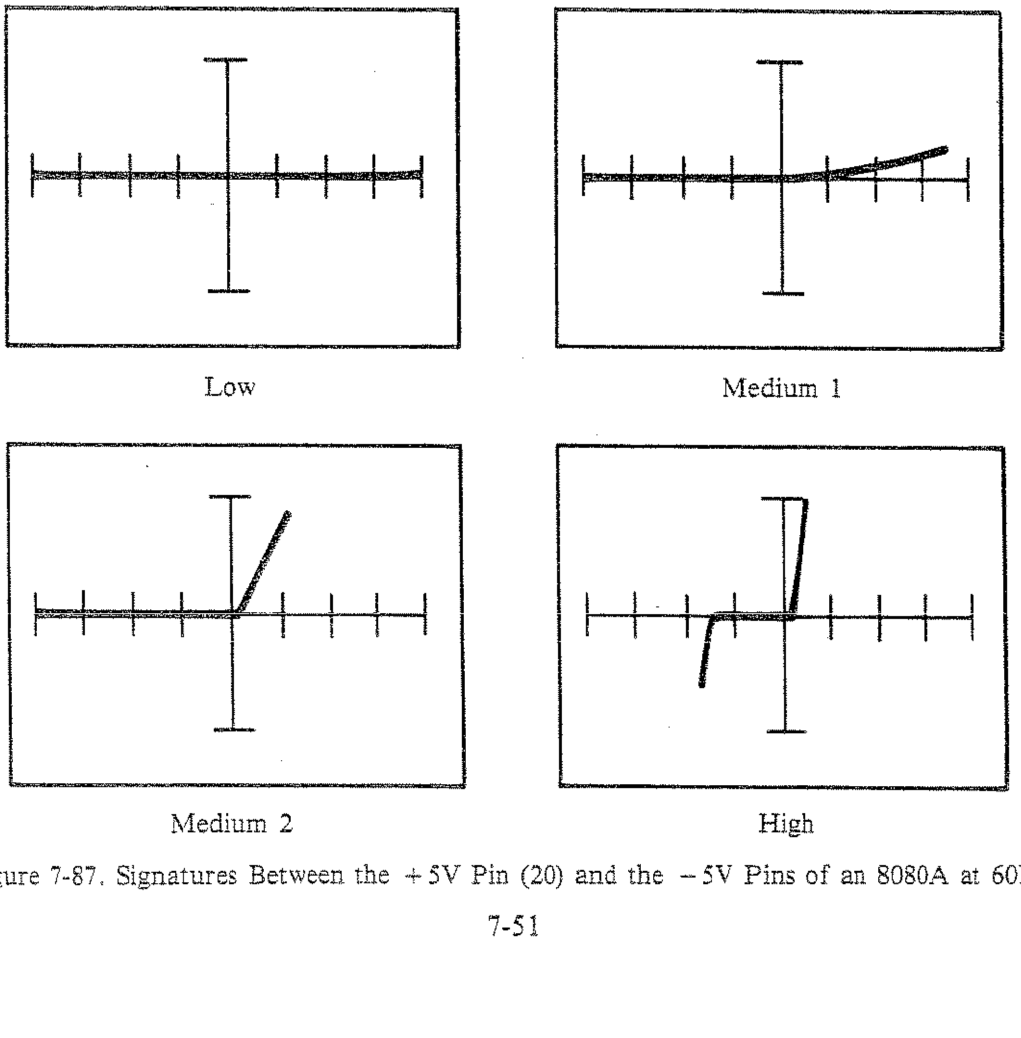


Figure 7-87. Signatures Between the +5V Pin (20) and the −5V Pins of an 8080A at 60Hz

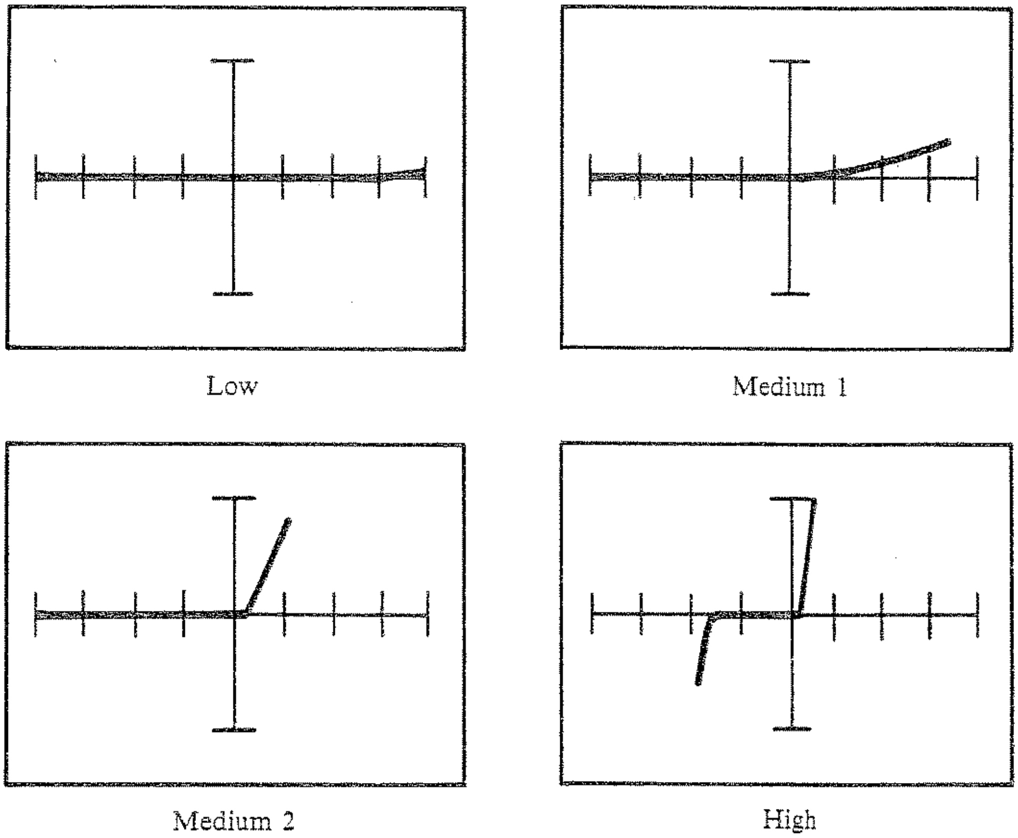


Figure 7-88. Signatures Between the +12V Pin (28) and the −5V Pin of an 8080A at 60Hz

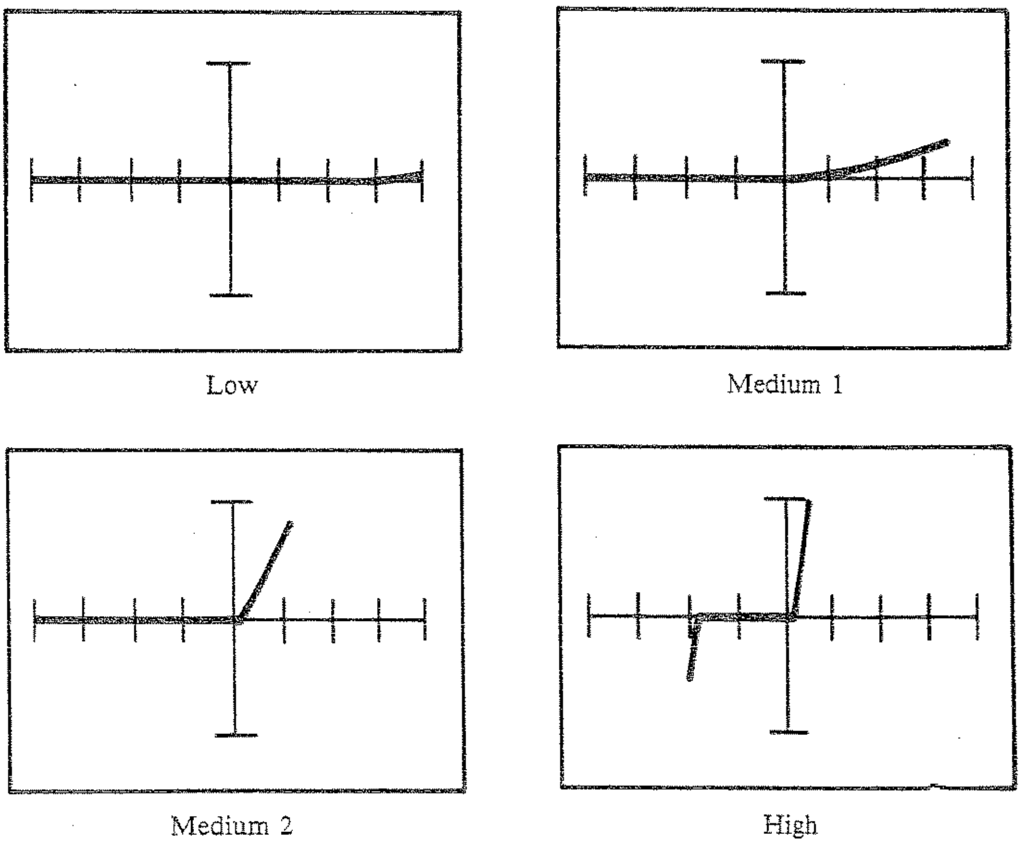


Figure 7-89. Signatures Between the INTE Pin (16) and the −5V Pin of an 8080A at 60Hz

SECTION 8
USING THE PULSE GENERATOR

8.1 INTRODUCTION

The previous sections have dealt with using the Tracker 2000 with two test leads to check components. This method is all that is necessary to test two terminal components, and yields useful information for many three terminal components as well. However, the Tracker 2000 has additional capability to test three terminal devices using the built-in pulse generator. The pulse generator provides a signal to the control input of a device while the normal test terminals of the Tracker 2000 are used to examine the outputs of the device. This method puts the device under test in its active region and a signature is produced that is the result of the device turning on and off. See section 2-6 for pulse generator operating instructions.

8.2 SILICON CONTROLLED RECTIFIERS (SCRs)

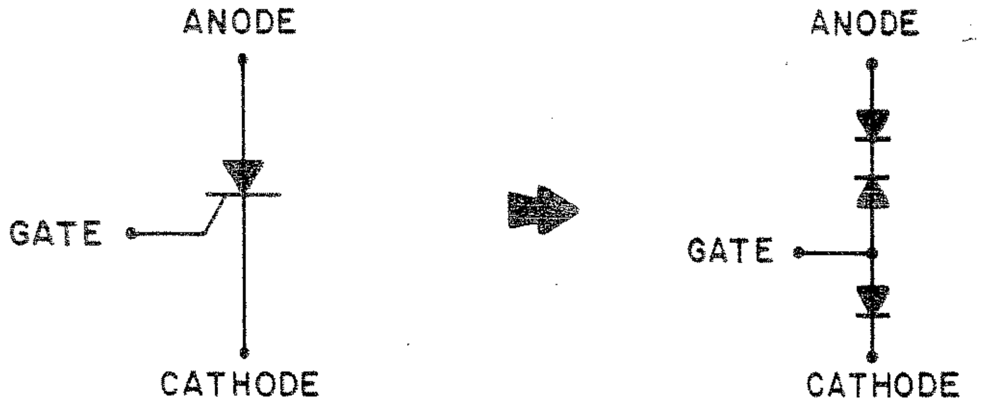


Figure 8-1. Silicon Controlled Rectifier

The symbol and equivalent circuit of a silicon controlled rectifier is shown in Figure 8-1. An SCR looks like a diode across its gate-cathode junction. If the Tracker 2000 is connected to the gate and cathode as shown in Figure 8-2, diode signatures appear on the display as shown in Figure 8-3. Note that the gate-cathode breakdown voltage can be observed.

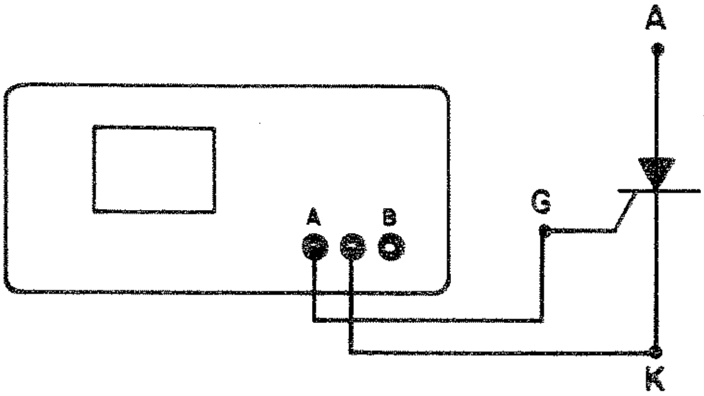
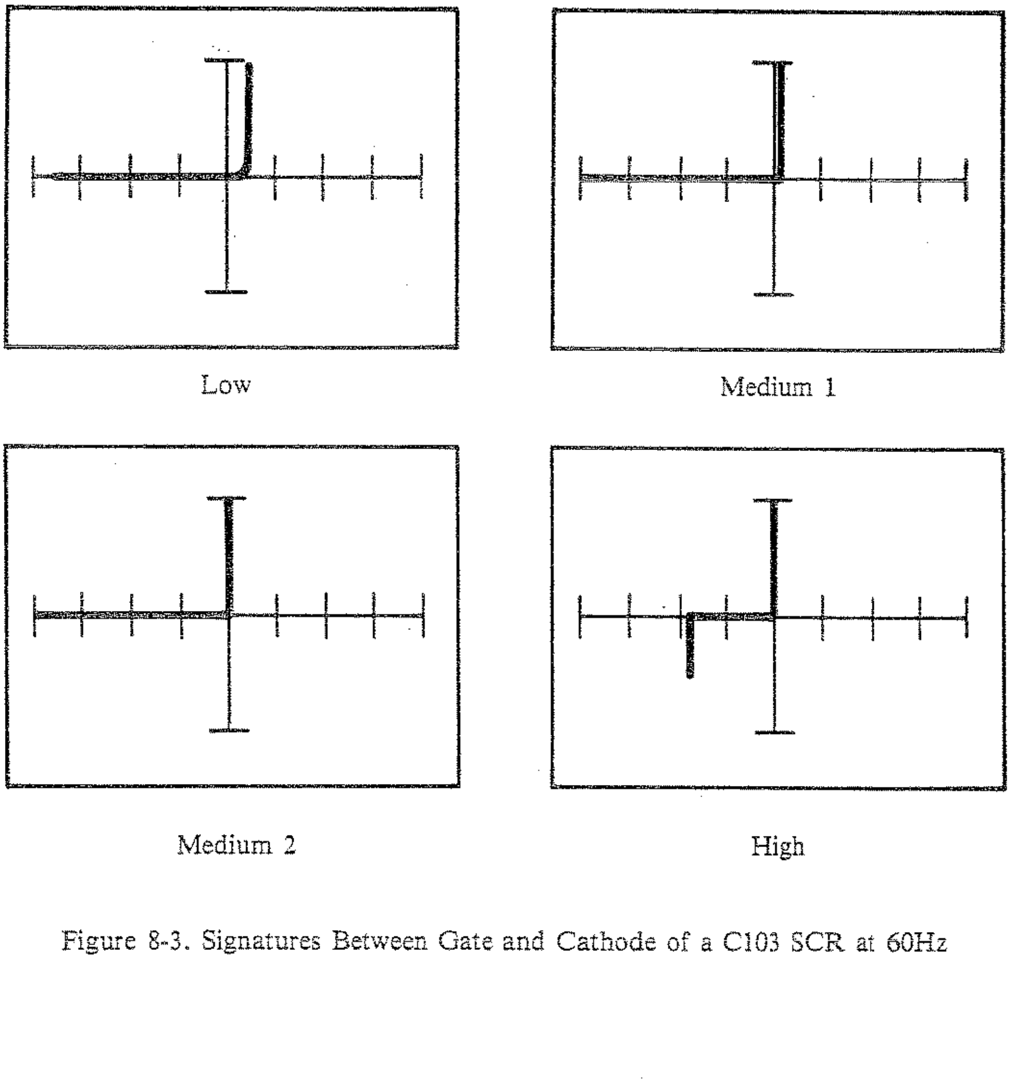


Figure 8-2. Gate-Cathode Test Connections



Low

Medium 1

Medium 2

High

Figure 8-3. Signatures Between Gate and Cathode of a C103 SCR at 60Hz

An SCR is like two diodes back to back across its gate-to-anode junction (See Figure 8-1). The Tracker 2000 displays these back to back diodes as an open circuit. Figure 8-4 shows the connections to test the anode and gate, while Figure 8-5 shows the connections to test the anode and cathode. The signatures for either connection are open circuit horizontal traces in all ranges (See Figure 8-6).

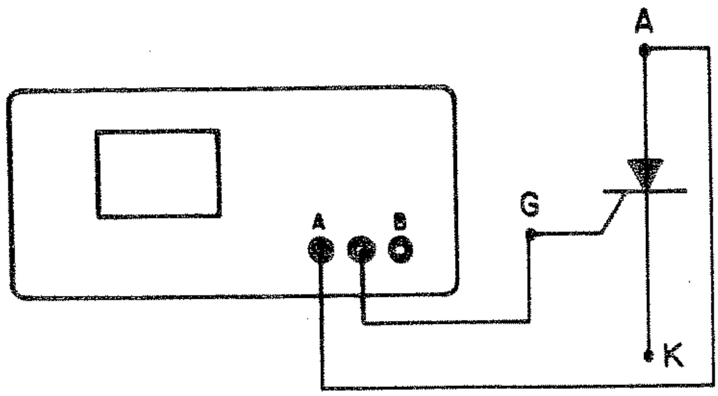


Figure 8-4. Anode-Gate Test Connections

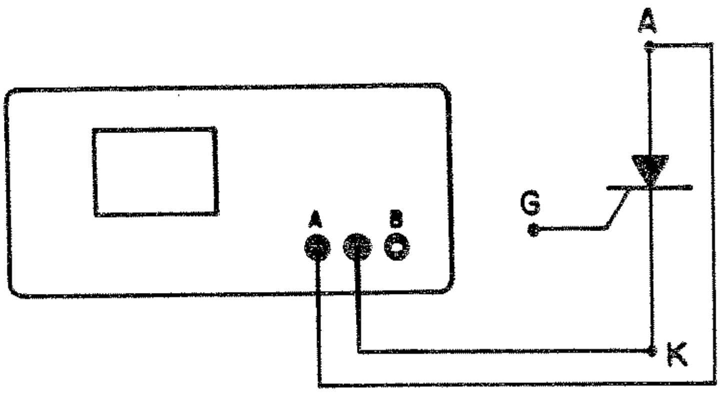
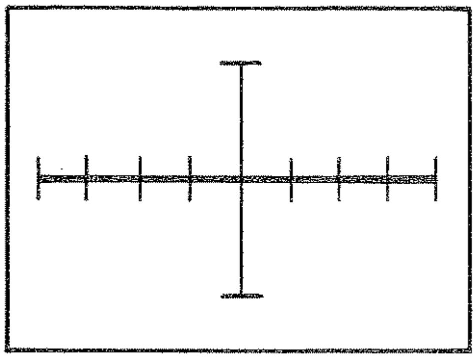


Figure 8-5. Anode-Cathode Test Connections



All Ranges

Figure 8-6. Signatures Between Anode-Gate or Anode-Cathode of a C103 SCR at 60Hz

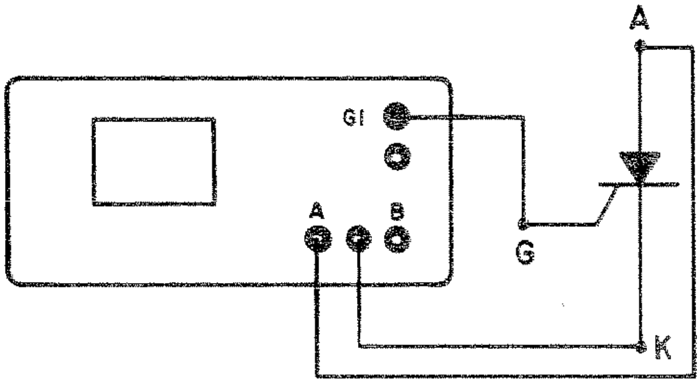


Figure 8-7. SCR Test Connections Using Pulse Generator

The pulse generator can drive the gate of an SCR as shown in the test circuit of Figure 8-7. With the Level control at zero, a horizontal trace is displayed (See Figure 8-8). This is expected since SCRs normally show an open circuit between anode and cathode or between anode and gate. Using DC stimulus (width = max), a point is reached as the level is increased where the SCR turns on, and the signature becomes like that of a diode. This is shown in Figure 8-9 for an SCR in all ranges.

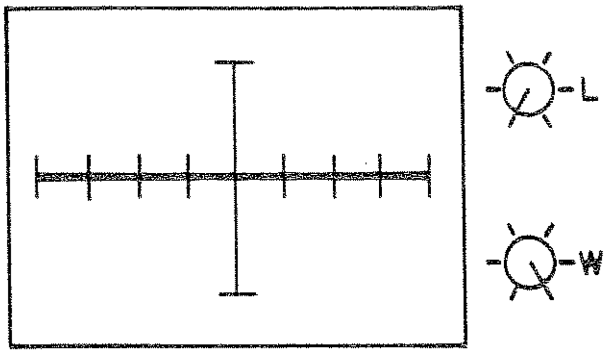


Figure 8-8. Zero Level All Ranges at 60Hz

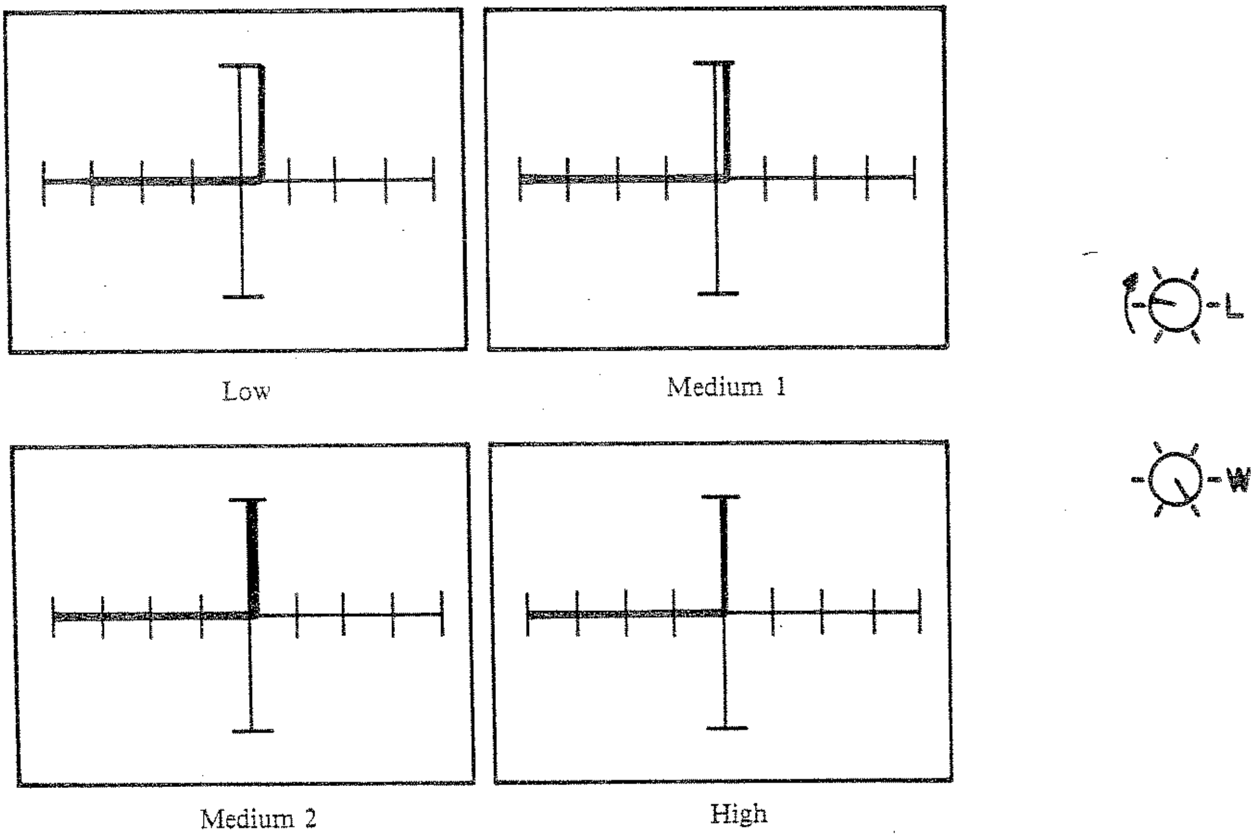
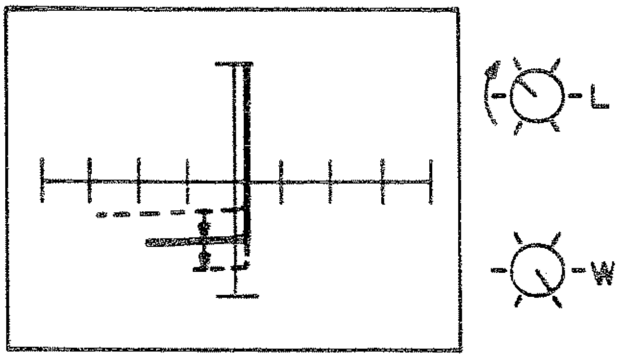


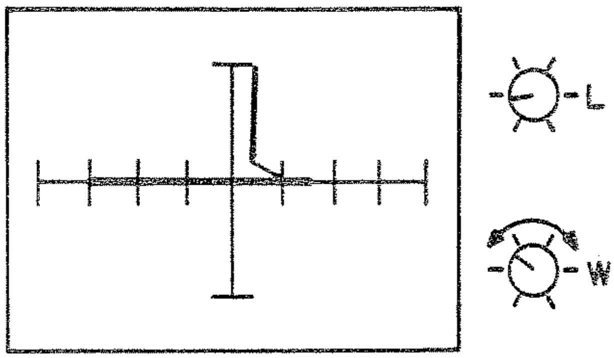
Figure 8-9. Effect of the Level Control (width = max) at 60Hz

In medium 1 range (or higher), if the level is increased beyond the point where the SCR turns on, the horizontal portion of the signature will begin to move downward as shown in Figure 8-10. This is due to a parasitic transistor action that exists outside the normal first quadrant operating parameters for an SCR. This effect is not especially relevant to determining whether an SCR is good or bad, and the user should simply note that it does not indicate a bad device. This effect is minimal in the low range.



Medium 1 Range, at 60Hz

Figure 8-10.



Low Range, at 60Hz

Figure 8-11.

The Width control can be varied over most of its range of adjustment without producing any change in the low range signature shown in Figure 8-11. This indicates a normal SCR that is switched on by any pulse that exceeds some minimum duration and remains in conduction until the anode-cathode signal changes polarity.

The best ranges for testing SCRs are the low and medium 1 ranges because those ranges have sufficient available current to produce normal action in many typical SCRs. In the medium 2 and high ranges, the maximum available current is much less than the minimum holding current of most SCRs and therefore the SCR switching characteristic cannot be observed.

8.3 TRIAC DEVICES

The triac is a bidirectional thyristor that was developed to extend the positive or negative supply of an SCR and to allow firing on either polarity with either positive or negative gate current pulses. Figure 8-12 shows the construction and symbol of a triac.

Apply the Tracker 2000 probes to the TRIAC 2N6070 as shown in Figure 8-13. Between gate and MT1, there are two diodes in parallel (See Figure 8-13b). The resulting signatures are shown in Figure 8-14.

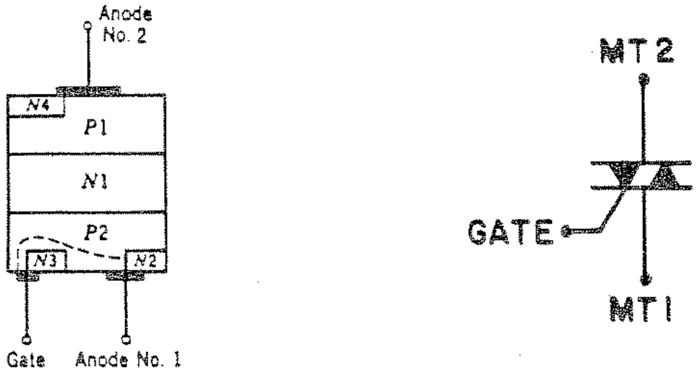
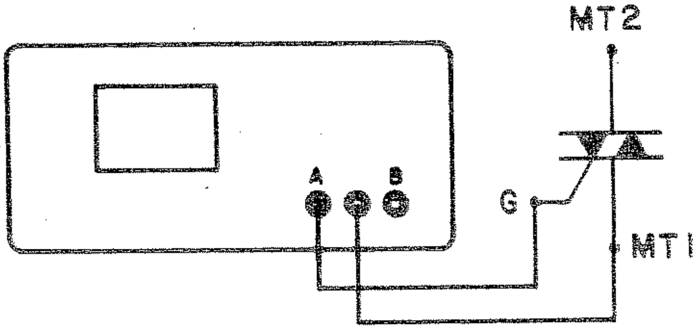
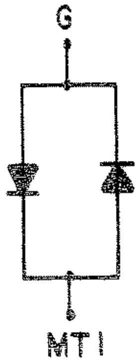


Figure 8-12. The Construction and Symbol of a Triac



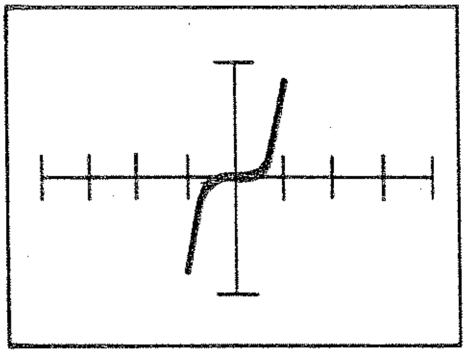
Gate-MT1 Test Connections

Figure 8-13a.

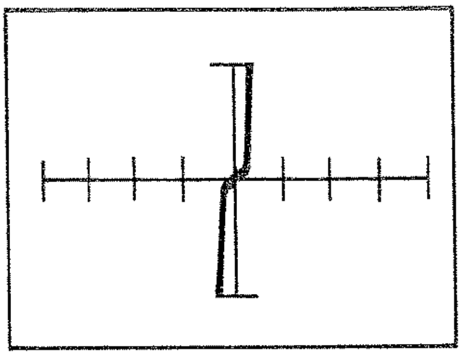


Gate-MT1 Equivalent Circuit

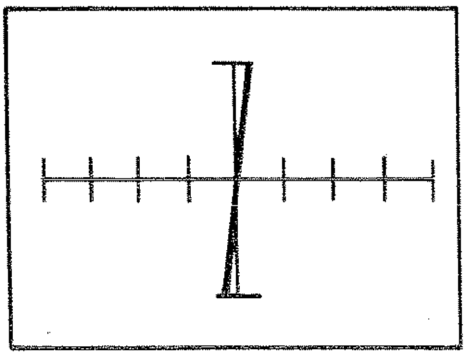
Figure 8-13b.



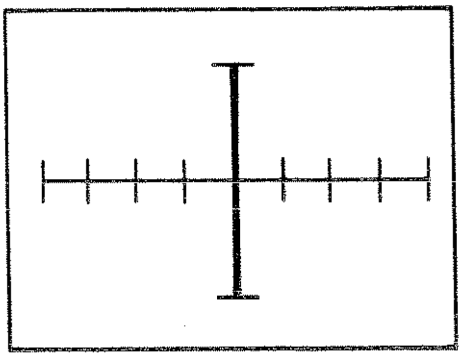
Low



Medium 1



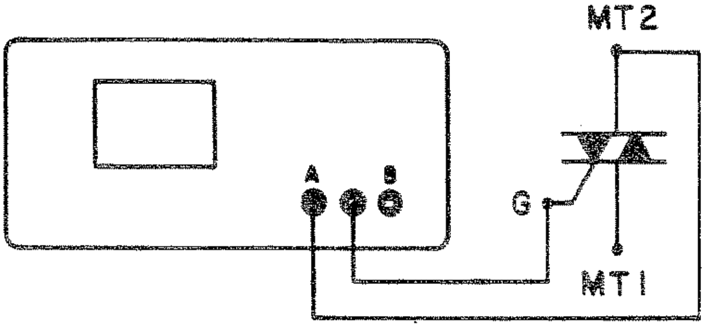
Medium 2



High

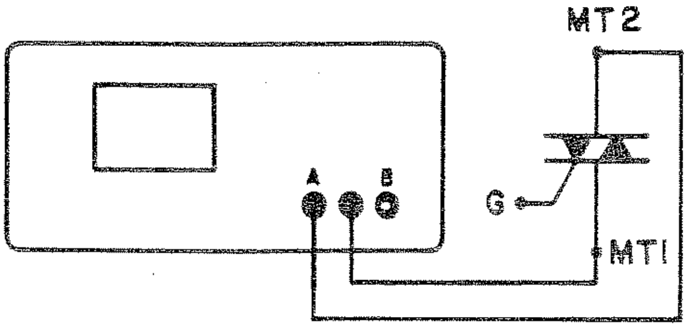
Figure 8-14. Signatures Between Gate and MT1 of a 2N6070 Triac, at 60Hz

Using either Figure 8-15a or Figure 8-15b as a triac test circuit, the Tracker 2000 should see an open circuit in all ranges as shown in Figure 8-16.



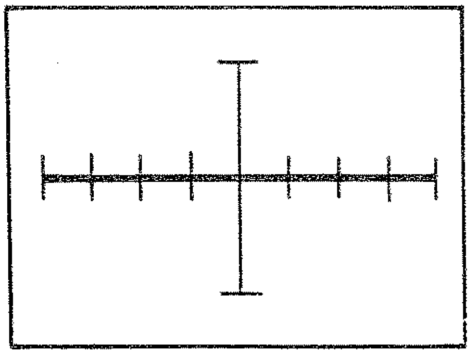
MT2-Gate Test Connections

Figure 8-15a.



MT2-MT1 Test Connections

Figure 8-15b.



All Ranges

Figure 8-16. Signatures Between MT2-Gate or MT1-MT2 of a 2N6070 to Triac at 60Hz

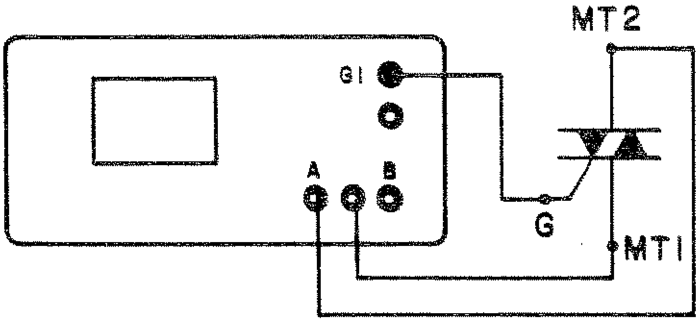


Figure 8-17. Triac Test Connections Using Pulse Generator

The test circuit for a triac using the pulse generator is shown in Figure 8-17. With the Level control at zero, an open circuit trace will be displayed. As the level is increased from zero (width = max) the triac will initially turn on in the first quadrant just like an SCR. Then with a slight increase in level, the triac turns on in the third quadrant also, which produces the back-to-back diode characteristic shown in Figure 8-18. This signature demonstrates the normal bidirectional conduction that is characteristic of a triac in the on state.

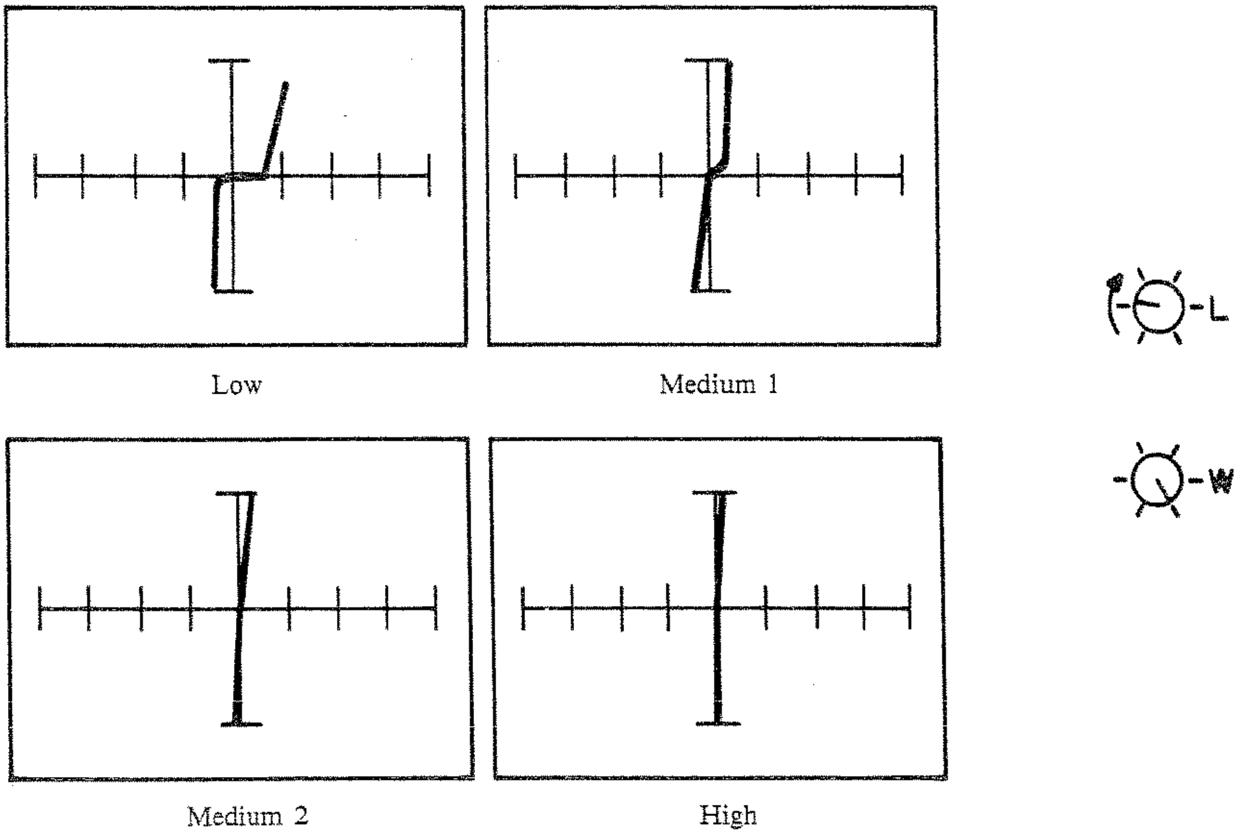
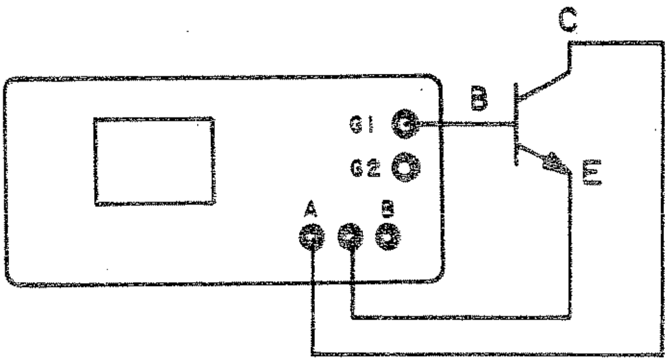


Figure 8-18. MT1-MT2 Signatures of a 2N6070 Triac with Gate Connected to Pulse Generator at 60Hz

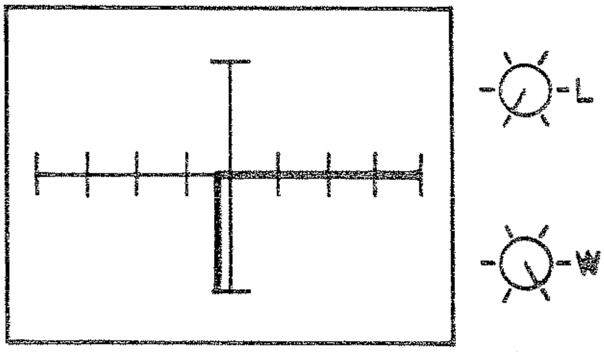
In all other ways, triacs are quite similar to SCRs. There is little change in the low range signature with various settings of the Width control once the triac has turned on, which verifies that a triac will continue to conduct after a pulse fires the gate. The medium 2 and high ranges have insufficient current to detect typical triac switching action and should not be used.

8.4 NPN TRANSISTORS

Figure 8-19a shows the test circuit for an NPN transistor using the pulse generator to drive the base. With the Level control at zero (fully counterclockwise), the display shows the signature in Figure 8-19b. This signature is the same as that for the collector-base junction of an NPN transistor in the medium 1 range. This is because the pulse generator output (G1) at zero level is equivalent to a 100 ohm resistor connected to common, and 100 ohms appears as a short circuit in that range.

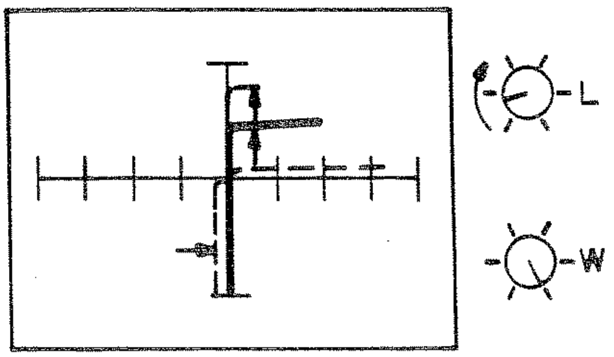


NPN Test Connections
Using the Pulse Generator
Figure 8-19a.



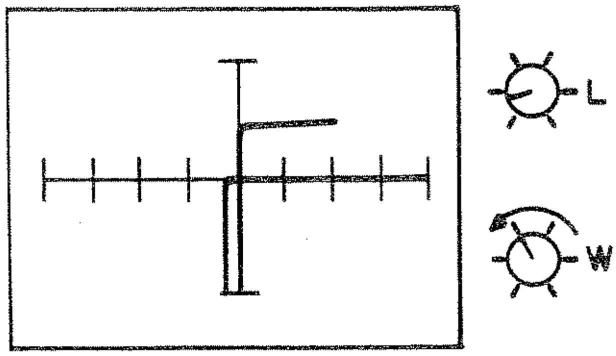
Medium 1 Range, at 60Hz
Figure 8-19b.

With the Width control turned fully clockwise, as the level is increased slowly from zero, the low impedance vertical line in the third quadrant will move towards and become even with the vertical axis, and then the "open circuit" horizontal line in the first quadrant will begin to move upward (see Figure 8-20a). This constant current signature is like that produced by a transistor curve tracer except that only one curve is shown instead of a family of curves. If the level is increased further, the horizontal portion of the signature will eventually move above the top end of the vertical axis. In the medium 1 range, the signature will then appear as a nearly vertical line indicating a low impedance.



Effect of the Level Control
(Width = Max)
Medium 1 Range, at 60Hz

Figure 8-20a.



Effect of the Width Control
at Constant level
Medium 1 Range, at 60Hz

Figure 8-20b.

The solid signature in Figure 8-20a is the result of DC stimulus. If the Width control is reduced from its maximum to about 40%, the signature shown in Figure 8-20b results. This display essentially shows the signatures of Figure 8-19b and 8-20a superimposed over one another with each one at half intensity. This composite signature means that the transistor is actually switching on and off with the pulse stimulus. Thus, the Tracker 2000 can test an NPN transistor in its active mode with either an AC or a DC stimulus using the pulse generator.

NOTE: This pulse generator cannot test PNP transistors in their active mode because it does not provide a negative stimulus.

8.5 OPTOCOUPLERS

The optocoupler (Optically Coupled Isolator, Photo-coupler) is a device designed for the transformation of electrical signals by utilizing optical radiant energy so as to provide coupling with electrical isolation between the input and the output.

These devices consist of a gallium arsenide infrared emitting diode and a silicon photo-device and provide high voltage isolation between separate pairs of input and output terminals. They include:

- Transistor optocoupler
- Darlington transistor optocoupler
- SCR optocoupler
- Triac optocoupler
- Photocell optocoupler

8.5.1 Transistor Optocoupler

The 4N25 transistor optocoupler consists of a gallium arsenide infrared light emitting diode coupled with a silicon phototransistor in a dual in line package.

Using the Tracker 2000 in the two terminal mode, some data about optocouplers can be learned. The input LED of the optocoupler can be tested as a stand alone diode with the test circuit shown in Figure 8-21. Figure 8-22 shows the signature of the LED part of a 4N25.

In a similar manner, the output NPN transistor can be tested by examining the signatures of base-emitter (Figure 8-23) and collector-emitter (Figure 8-24).

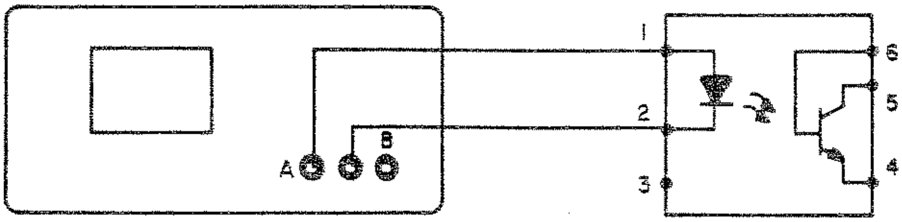


Figure 8-21. Test Circuit for Input LED of 4N25

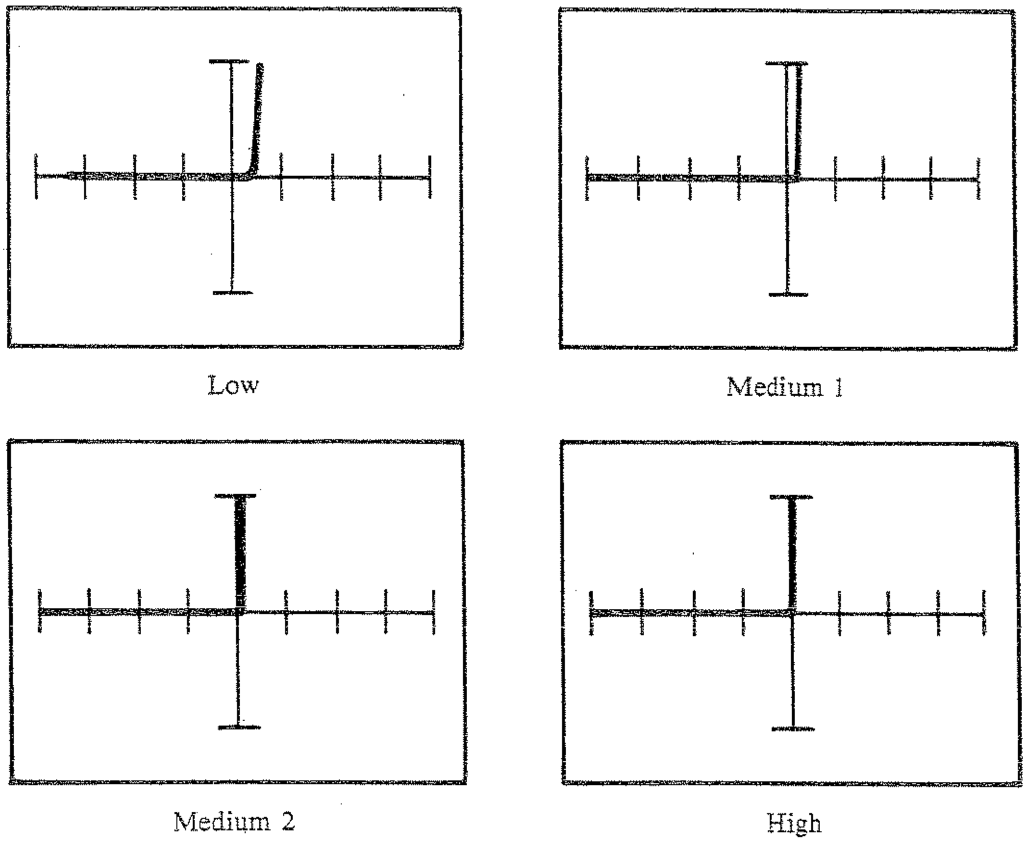


Figure 8-22. Signatures of the LED of a 4N25 at 60Hz

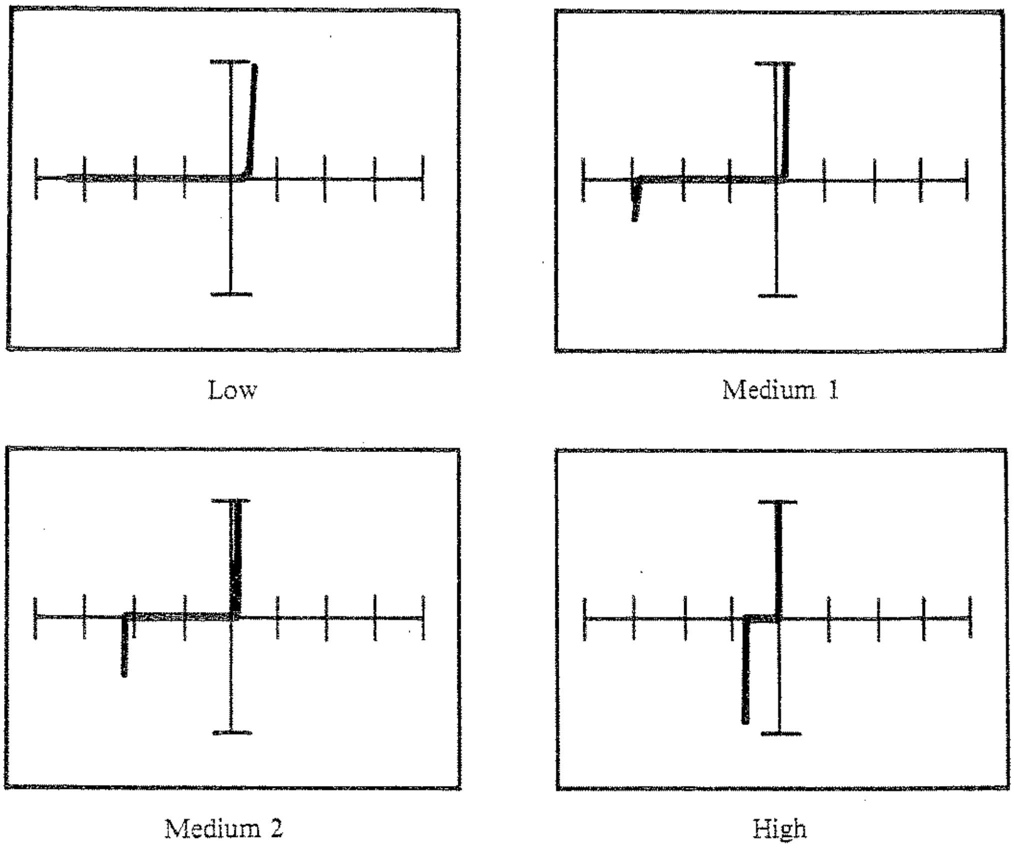


Figure 8-23. Signatures of the Base-Emitter of a 4N25 at 60Hz

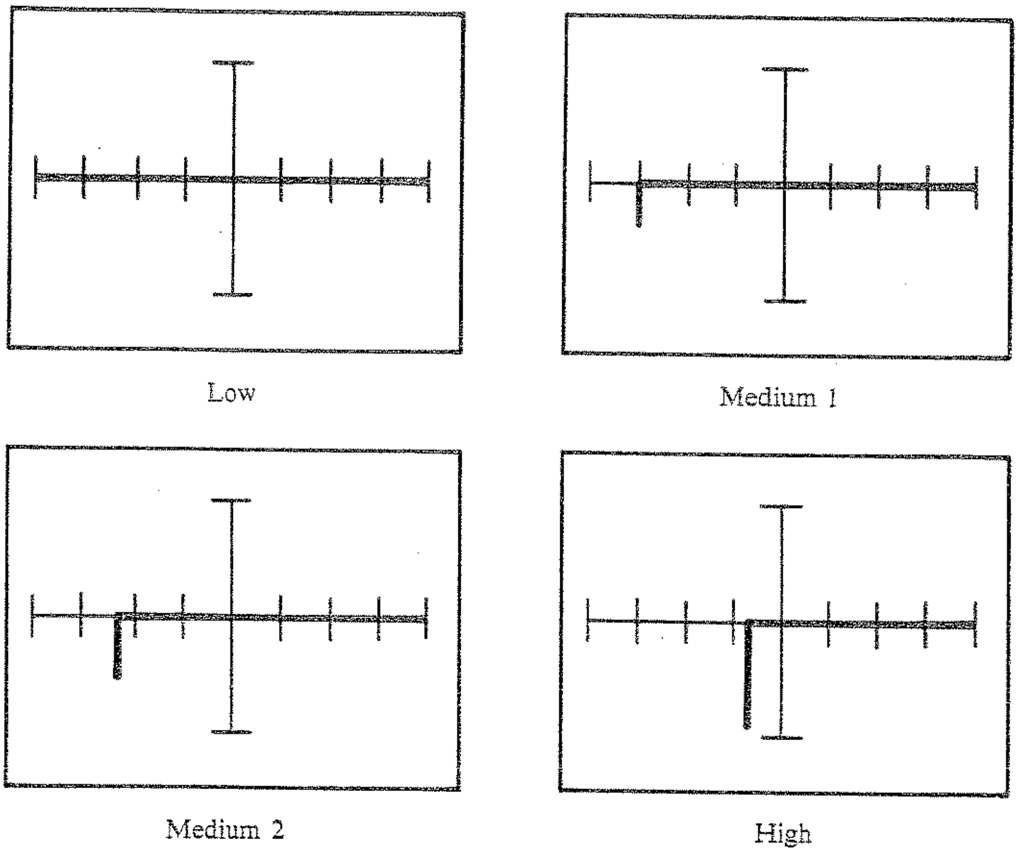


Figure 8-24. Signatures of the Collector-Emitter of a 4N25, at 60Hz

These two terminal techniques can check the LED and the phototransistor, but they cannot verify the optical link between the two devices. This is why the optocoupler is uniquely suited to testing in the three terminal mode of the Tracker 2000.

Figure 8-25 shows the test connections to an optocoupler using the pulse generator. The optocoupler shown has an NPN phototransistor as its output device, and is representative of a large percentage of the optocouplers used in modern electronic equipment. The user should note that pin 2 and pin 4 need to be connected with a jumper to establish a common point for the Tracker 2000.

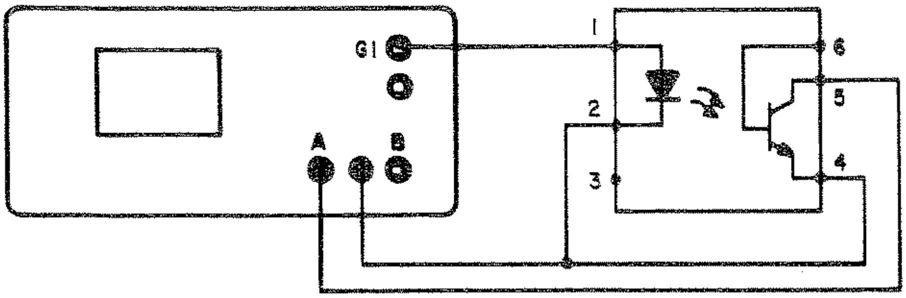
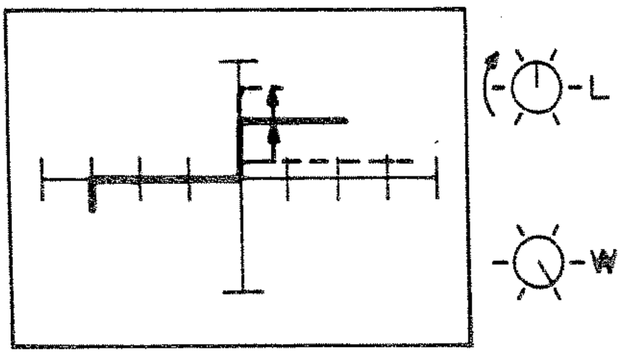


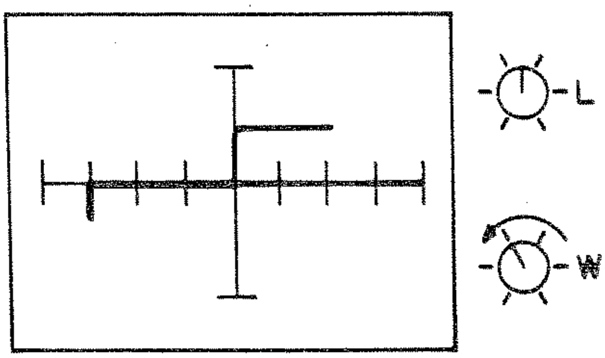
Figure 8-25. Optocoupler Test Connections Using Pulse Generator

Using the test circuit in Figure 8-25, if the Level control is at zero and the Width control is at maximum, the same signature is produced that was shown in Figure 8-24. This is not unexpected since there is zero drive to the LED and therefore, zero base current in the phototransistor. As the level is increased from zero, the horizontal portion of the trace in the first quadrant will move upward just like an NPN transistor driven directly by the pulse generator (see Figure 8-26a). There are two main differences between the transistor driven directly and the optocoupler transistor. First, the Level control does not affect the signature in the third quadrant with the optocoupler under test, whereas the transistor with direct drive has a different signature in the third quadrant and it moves as the Level control is increased. Second, the sensitivity of the first quadrant signature to the position of the Level control is much lower with the optocoupler than with the transistor. This is because of the optocoupler parameter known as "current transfer ratio" or CTR which is the ratio of collector current in the phototransistor to the forward current in the LED. CTR for common optocouplers is approximately one, whereas the corresponding parameter for the transistor alone is the forward current gain (beta) which is usually in the range from 50 to 200. This accounts for the decreased Level control sensitivity when testing optocouplers.



Effect of the Level Control
(Width = Max)
Medium 1 Range at 60Hz

Figure 8-26a.



Effect of the Width Control
at a Constant Level
Medium 1 Range at 60Hz

Figure 8-26b.

The optocoupler can be tested with an AC stimulus by turning the Width control to approximately 40% duty cycle. The resulting composite signature is equivalent to the signatures of Figure 8-24 (Medium 1 Range) and 8-26a superimposed on each other. The first quadrant curves are at half intensity due to the switching action caused by the pulse generator, while the third quadrant is at full intensity because the pulse generator does not affect the signature there.

Using the second pulse generator output and the Alternate mode, two devices of the same type can be checked and compared to each other. The test connections for this method are shown in Figure 8-27.

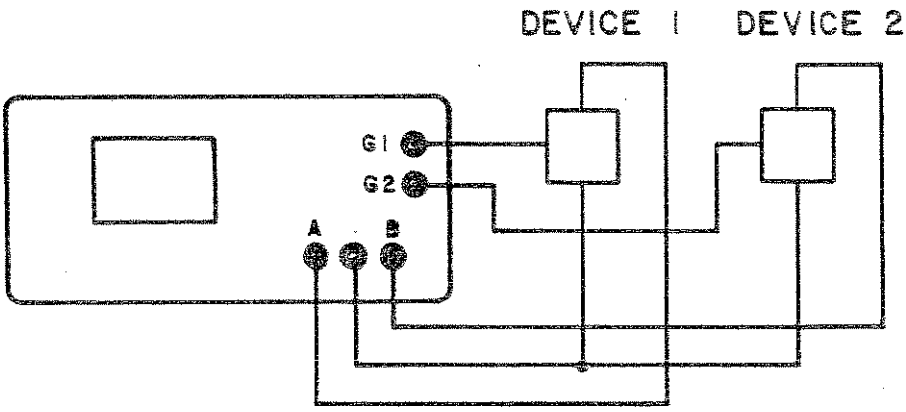


Figure 8-27. Pulse Generator Comparison Mode

8.5.2 Darlington Transistor Optocoupler

The darlington transistor optocoupler consists of a gallium arsenide infrared light emitting diode coupled with a silicon photodarlington transistor in a dual-in-line package. Figure 8-28 shows the pin configuration of a 4N31 darlington transistor optocoupler. The darlington adds the effects of an additional stage of transistor gain to the transistor optocoupler. The two terminal test mode of a 4N31 is similar to that of 4N25 discussed in last section, and its signatures are shown in Figure 8-29 through 8-31.

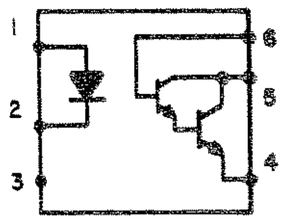
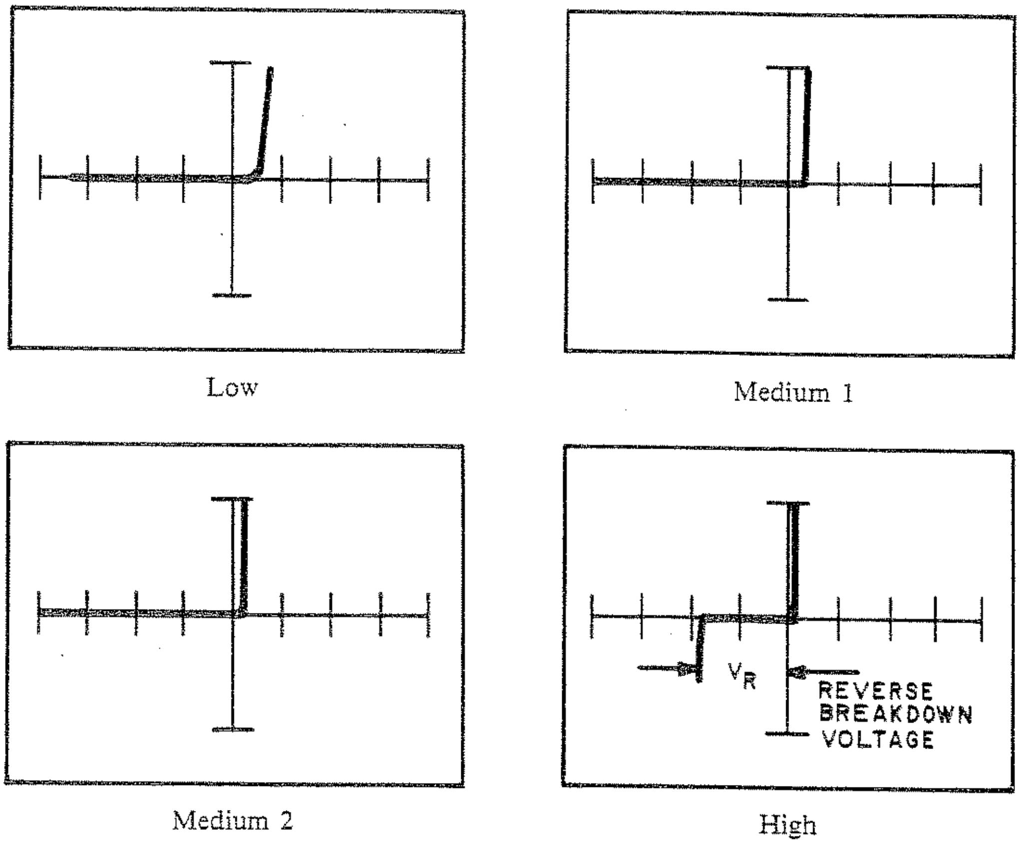
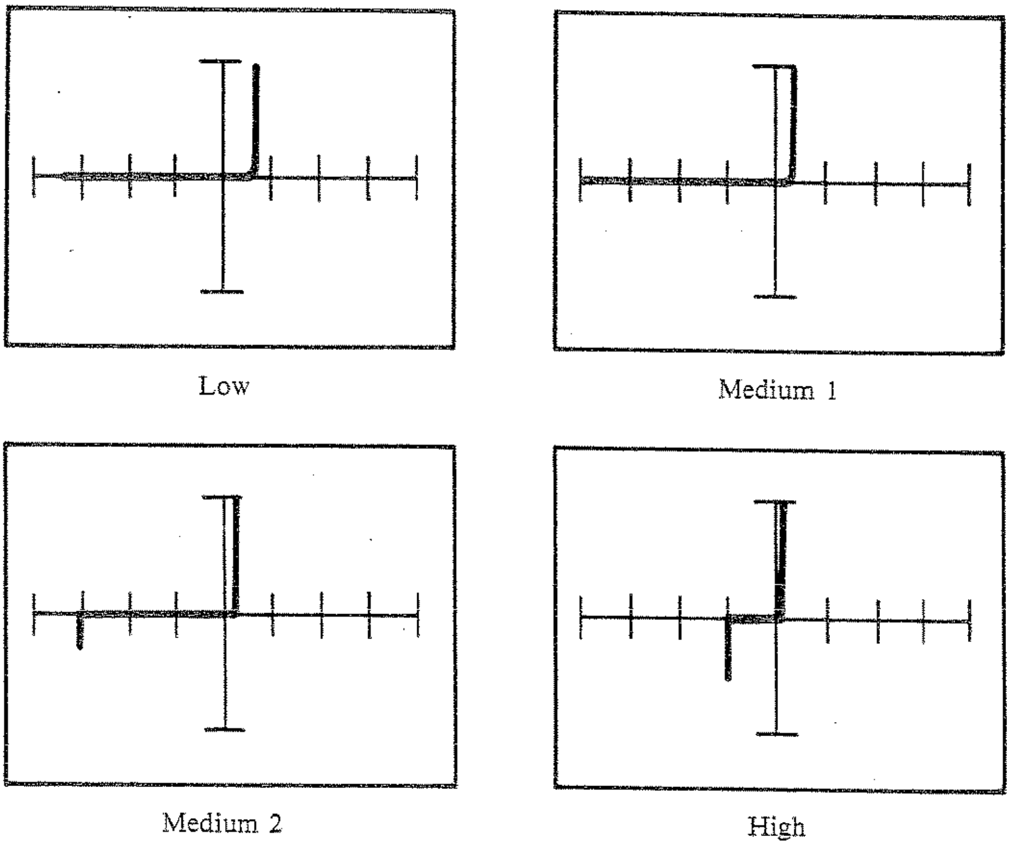


Figure 8-28. Pin Configurations of a 4N31 Darlington Transistor Optocoupler



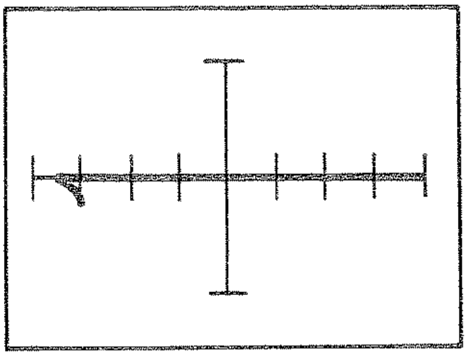
Low
Medium 1
Medium 2
High

Figure 8-29. Signatures of the LED Part of a 4N31 at 60Hz

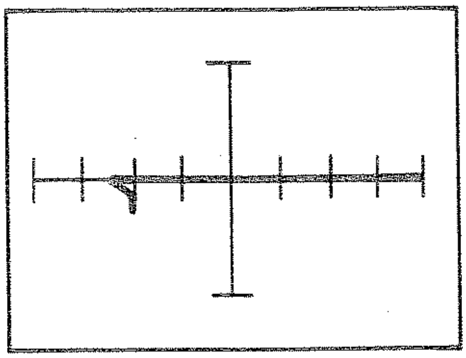


Low
Medium 1
Medium 2
High

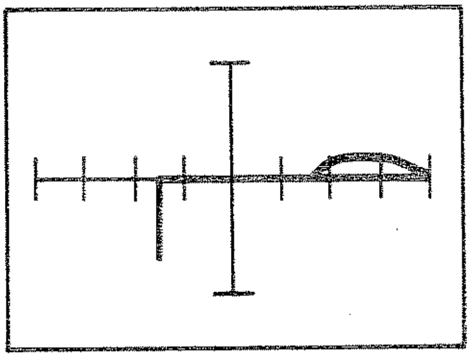
Figure 8-30. Signatures of the Base-Emitter of a 4N31 at 60Hz



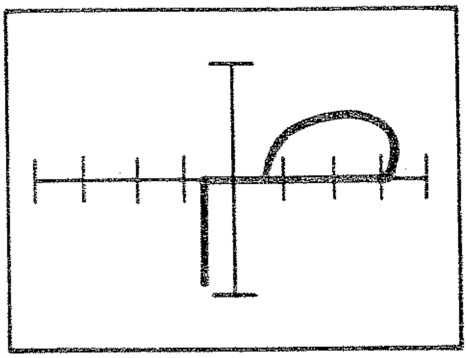
Low



Medium 1



Medium 2



High

Figure 8-31. Signatures of the Collector-Emitter of a 4N31 at 60Hz

The loops that appear in the medium 2 and high range signatures in Figure 8-31 are caused by a 60Hz signal picked up by the base of the darlington transistor.

Testing a 4N31 with the pulse generator:

The test circuit is shown in Figure 8-32

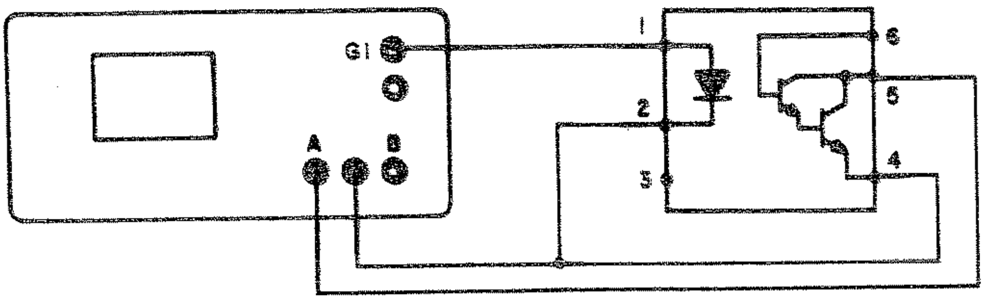


Figure 8-32. Test Circuit for a 4N31 with the Pulse Generator

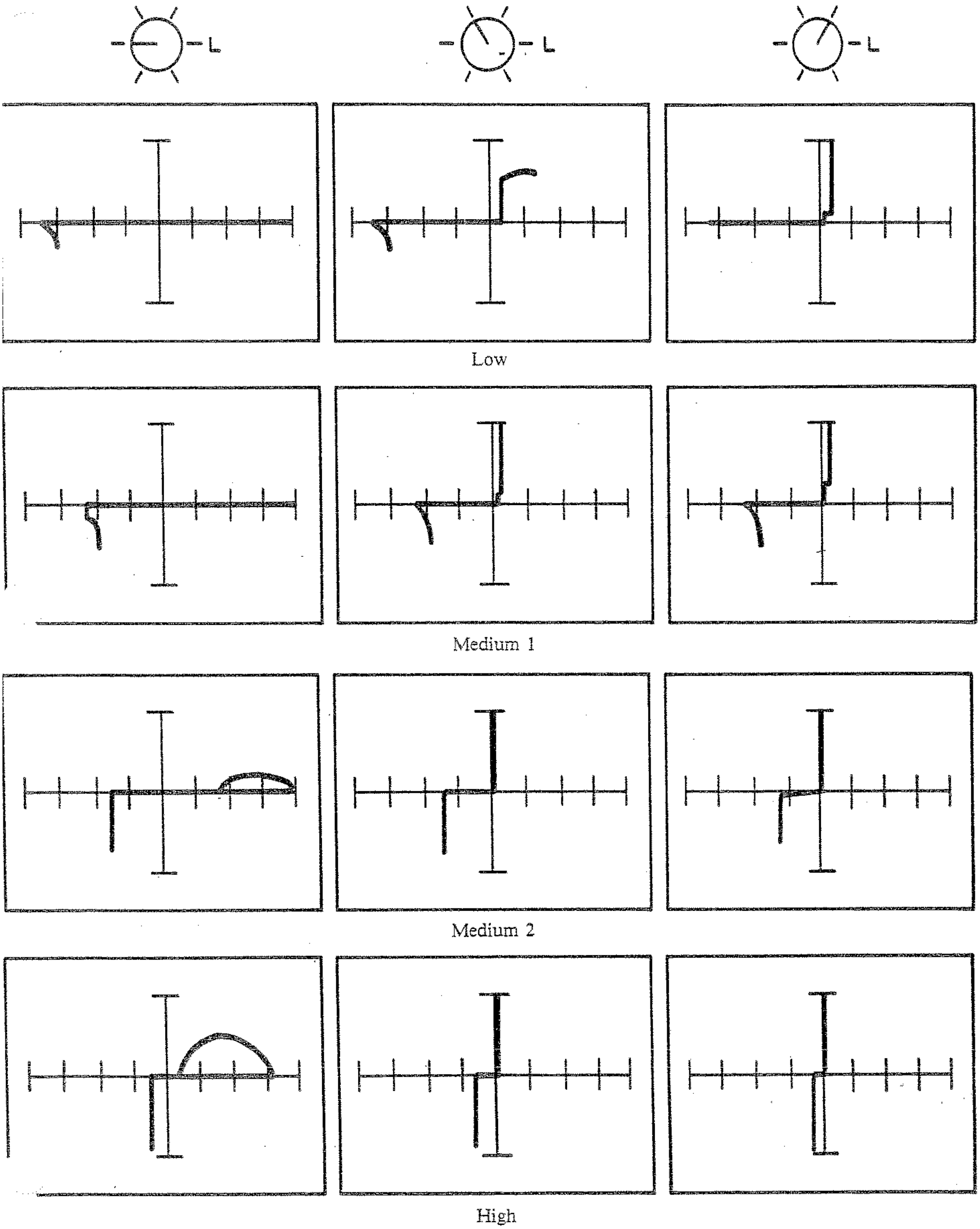


Figure 8-33. Signature variations of a 4N31 as a function of pulse level (maximum pulse width) at 60Hz

8.5.3 SCR Optocoupler

The GE H11C3 (for pin configuration see Figure 8-34) consists of a gallium arsenide infrared light emitting diode coupled with a light activated Silicon Controlled Rectifier in a dip package.

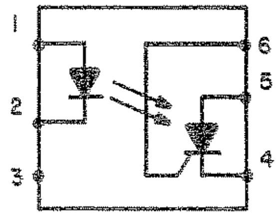


Figure 8-34. Pin configuration of a H11C3 SCR Optocoupler

Figures 8-35 through 8-37 show the two terminal test mode signatures of a H11C3.

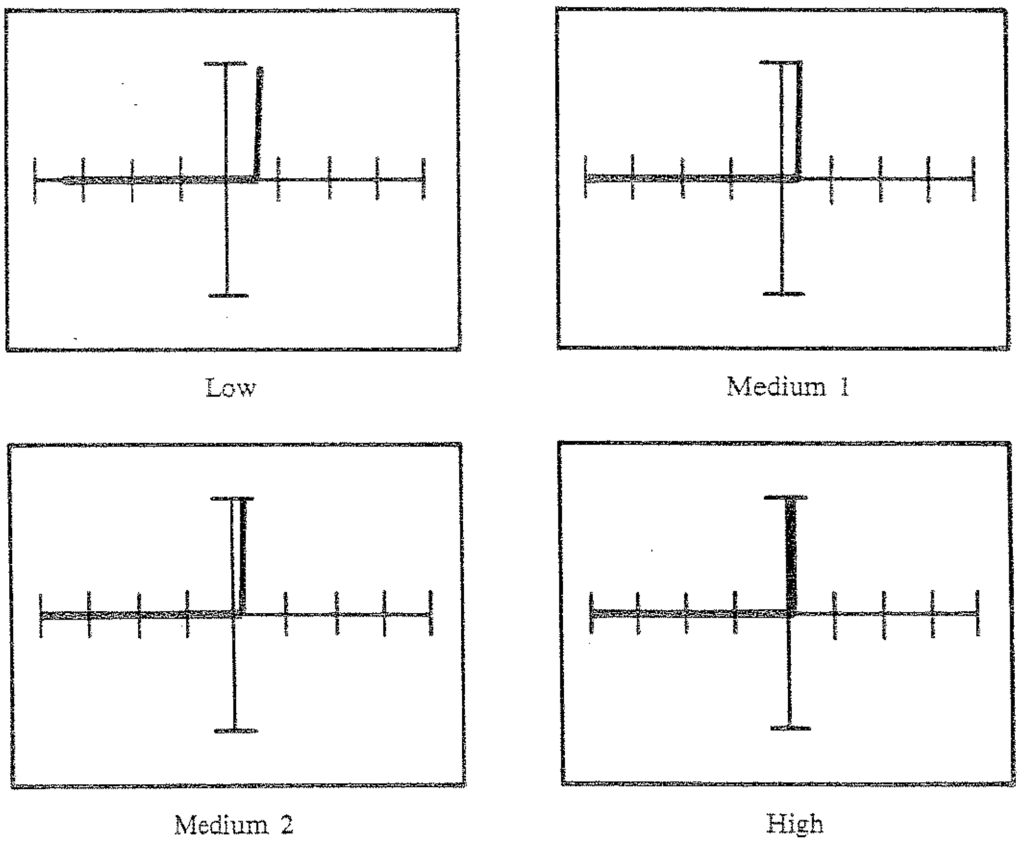
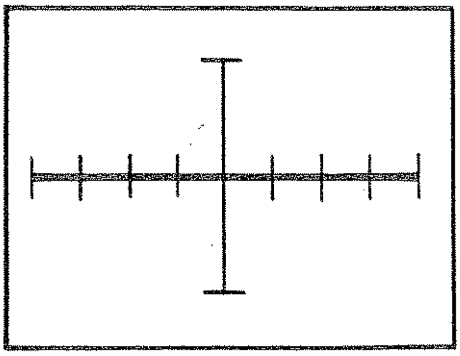
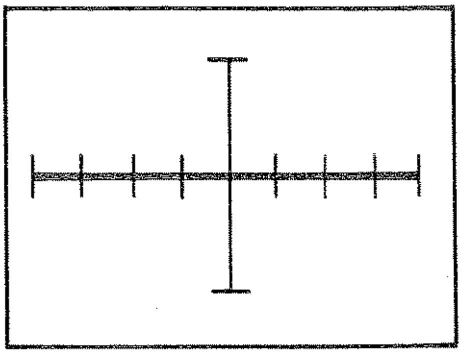


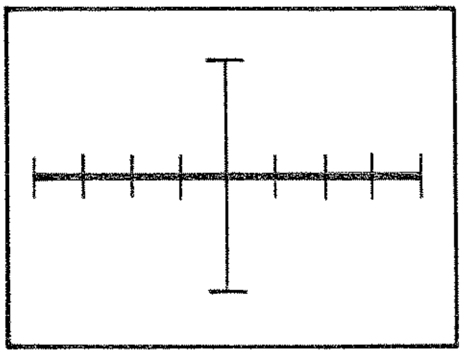
Figure 8-35. Signatures of the LED part of a H11C3 at 60Hz



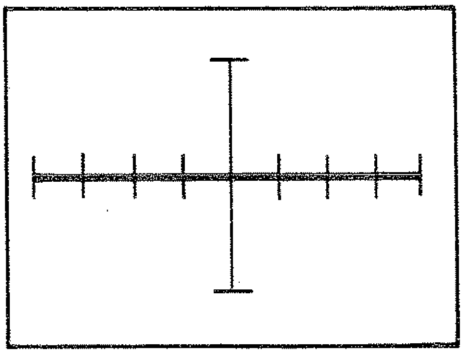
Low



Medium 1

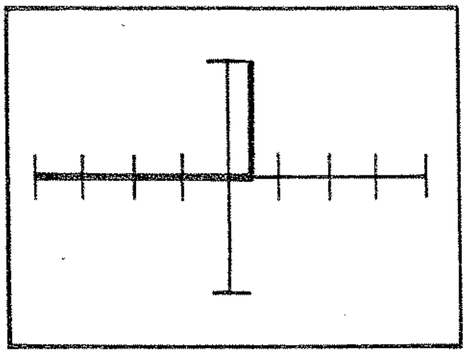


Medium 2

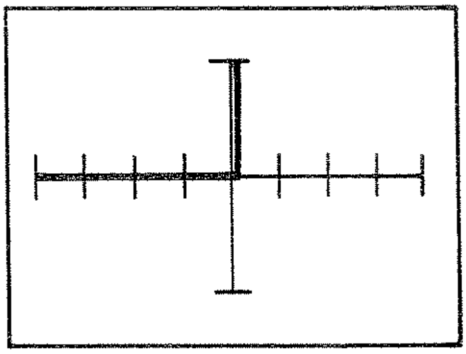


High

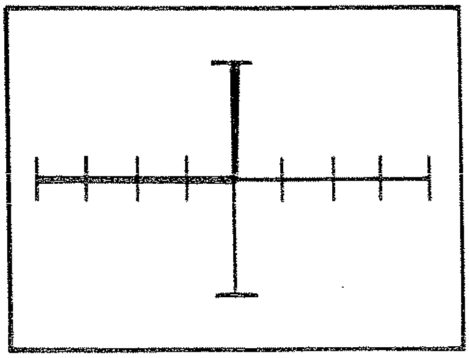
Figure 8-36. Signatures Between Cathode and Anode (Pin 4 and Pin 5) of a H11C3 at 60Hz



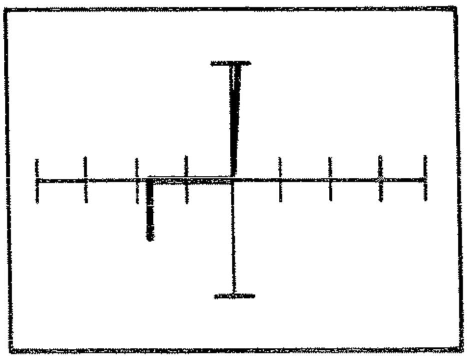
Low



Medium 1



Medium 2



High

Figure 8-37. Signatures Between Gate and Cathode (Pin 6 and Pin 4) of a H11C3 at 60Hz

Testing a H11C3 with the pulse generator:

The test circuit for a H11C3 is shown in Figure 8-38.

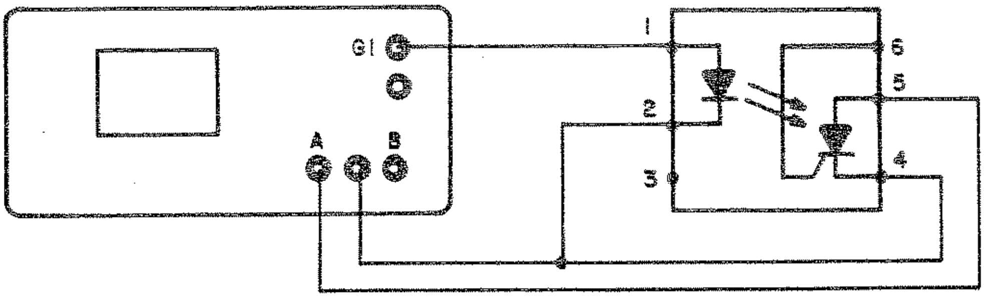


Figure 8-38. Test Circuit for a H11C3 with Pulse Generator

The dynamic test signatures for a H11C3 are shown in Figure 8-39 for various settings of pulse level at maximum pulse width. Different settings of pulse level and pulse width will give different signatures.

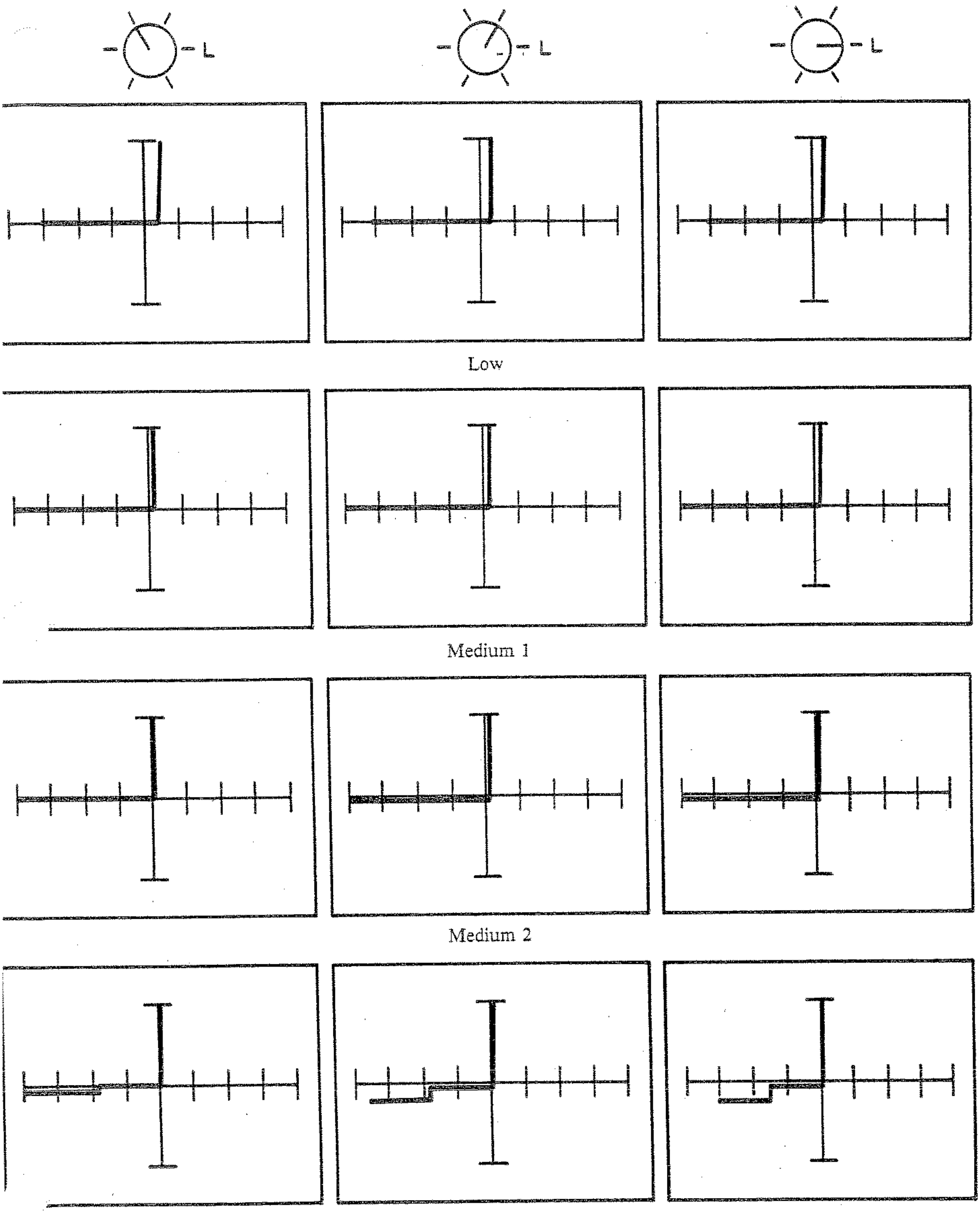


Figure 8-39. Signature variations of a H11C3 as a function of pulse level for the maximum pulse width, at 60Hz.

8.5.4 Triac Optocoupler

The Motorola MOC3010 (for pin configurations see Figure 8-40) consists of a gallium arsenide infrared light emitting diode coupled with a light activated triac in a dip package.

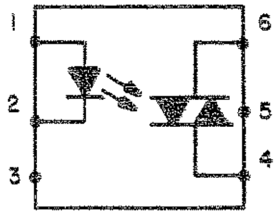


Figure 8-40. Pin Configurations of a MOC3010 Triac Optocoupler

The two terminal test mode signatures of a MOC3010 are shown in Figure 8-41 through Figure 8-42.

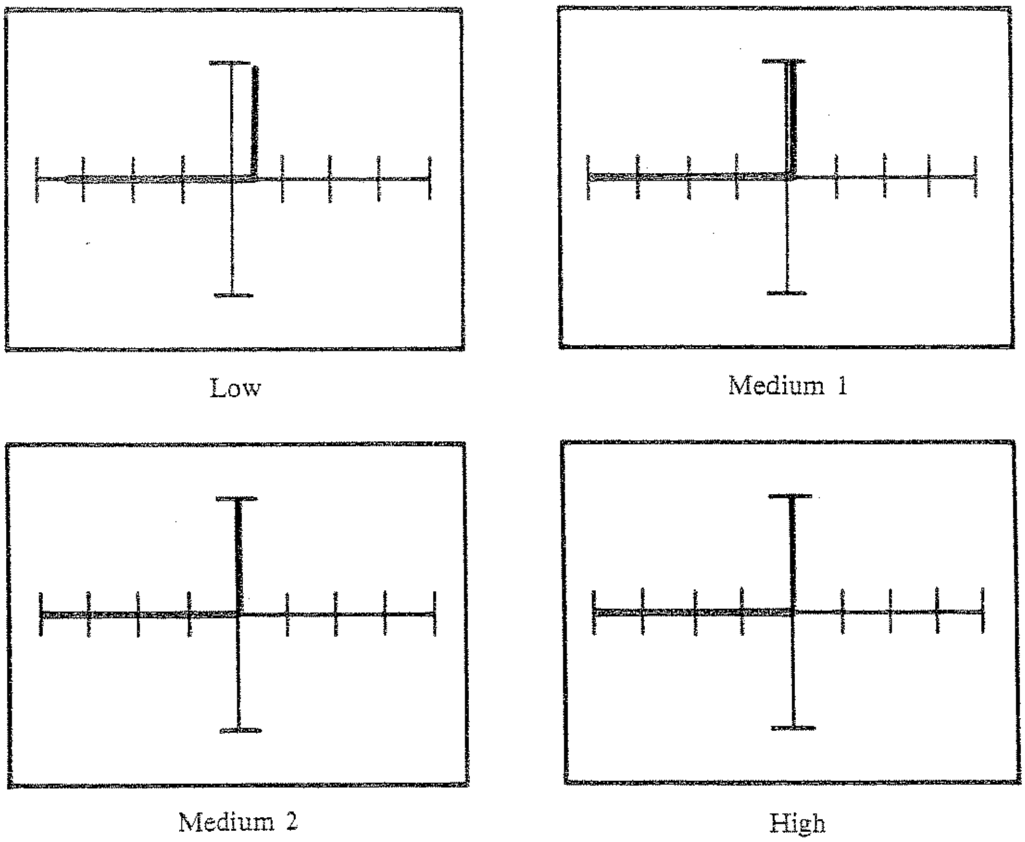
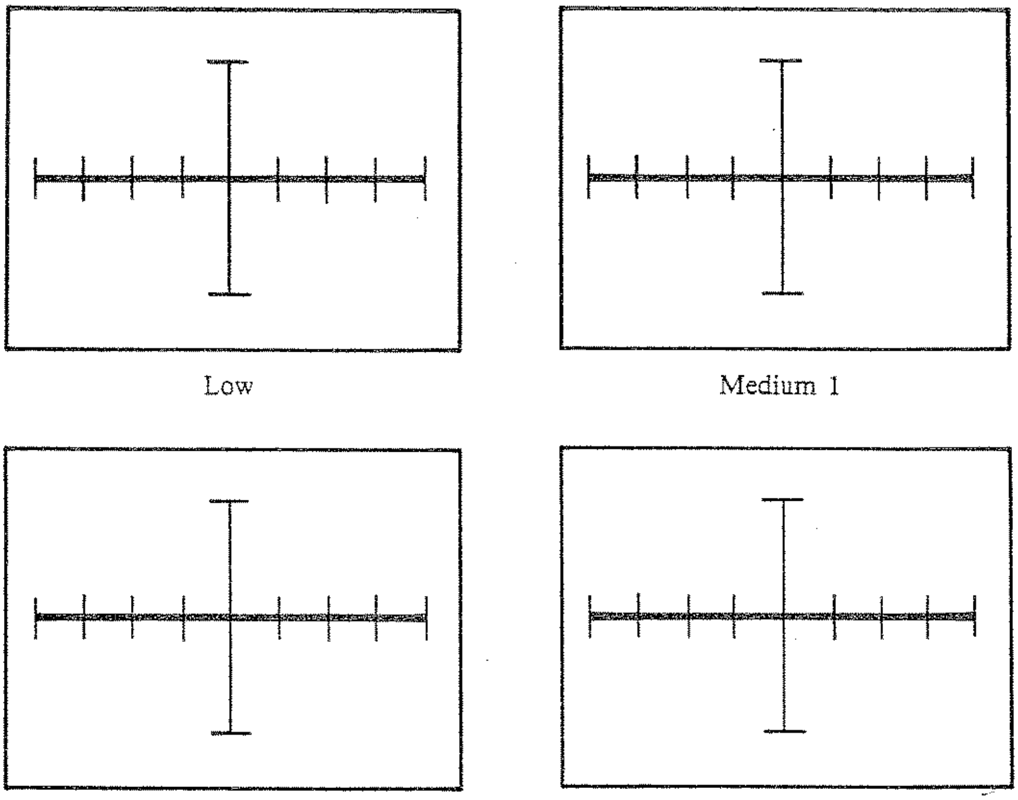


Figure 8-41. Signatures of the LED part (Pin 1 and Pin 2) of a MOC3010, at 60Hz.



Low

Medium 1

Medium 2

High

Figure 8-42. Signatures of the Triac Part (Pin 6 and Pin 4) of a MOC3010, at 60Hz.

Testing a MOC3010 with the pulse generator:

The test circuit with the pulse generator for a MOC3010 is shown in Figure 8-43.

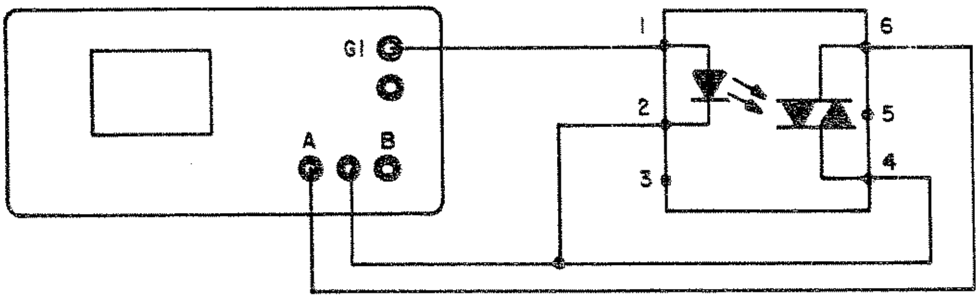


Figure 8-43. Pulse Generator Test Circuit for a MOC3010 Triac Optocoupler.

The dynamic test signatures for a MOC3010 are shown in Figure 8-44 for various settings of the pulse level at maximum pulse width. Different settings of pulse level and pulse width will give different signatures.

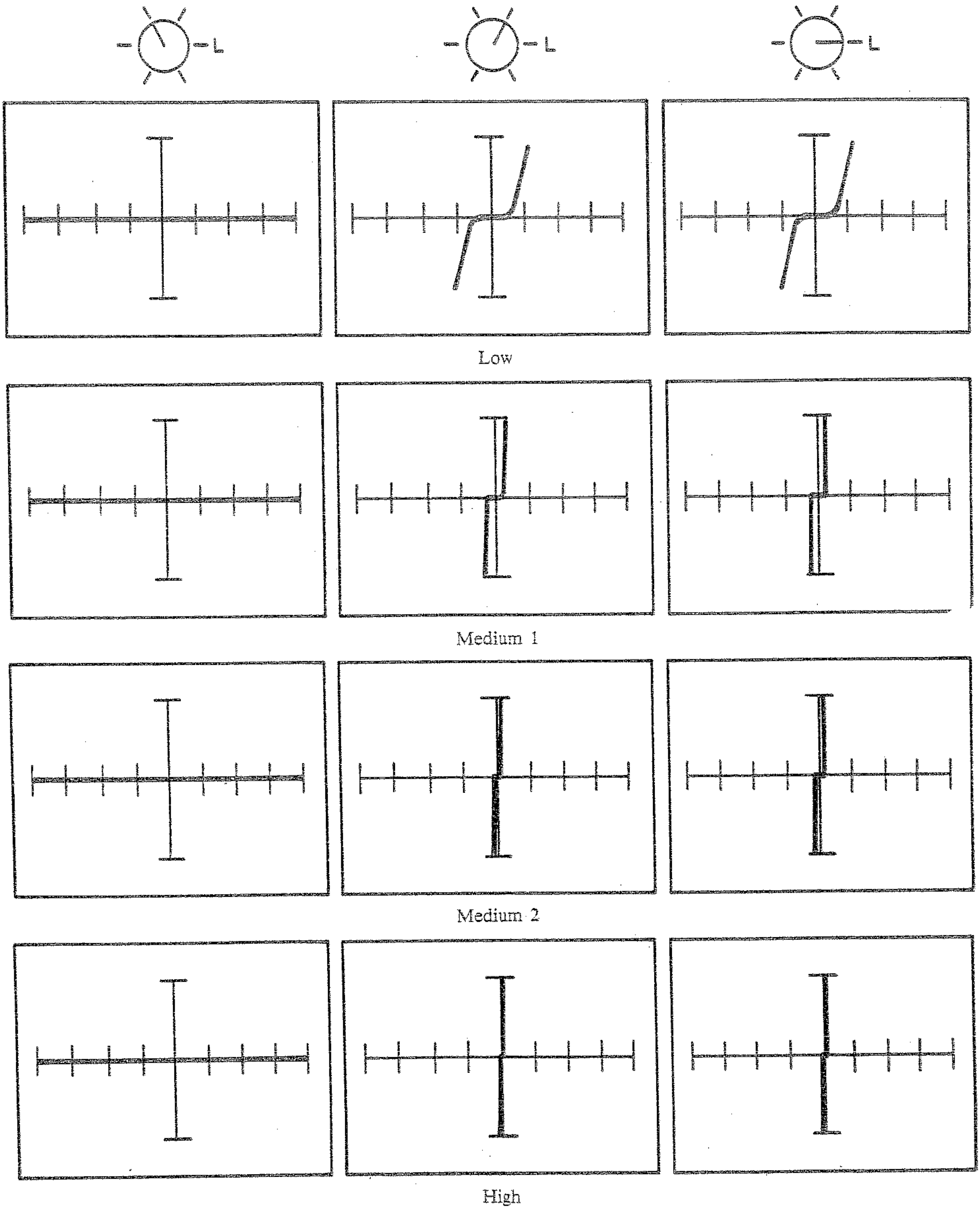


Figure 8-44. Signature Variations of a MOC3010 as a Function of the Pulse Level (maximum pulse width) at 60Hz

8.5.5 Photocell Optocoupler

The Clairex CLM-51 photocell optocoupler consists of a gallium arsenide infrared light emitting diode coupled to a symmetrical bilateral photoconductive cell. The cell is electrically isolated from the input. Figure 8-45 shows the pin configuration of a CLM-51. The off resistance of the cell is in excess of 1 megohm, thus it appears as an open circuit to the Tracker 2000.

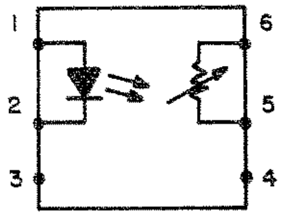
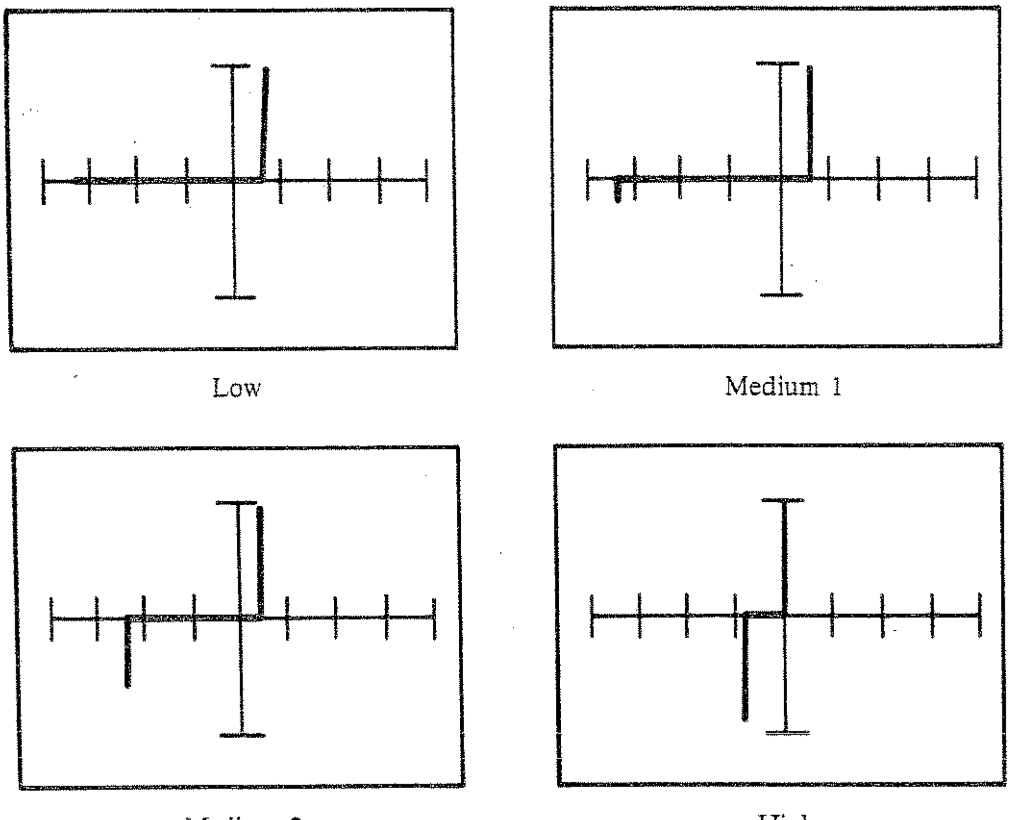


Figure 8-45. Pin Configurations of a CLM-51 Photocell Optocoupler.

The two terminal mode signatures of a CLM-51 are shown in Figure 8-46 and Figure 8-47.



Low | Medium 1 | Medium 2 | High

Figure 8-46. Signatures of the LED part (Pin 1 and Pin 2) of a CLM-51 at 60Hz

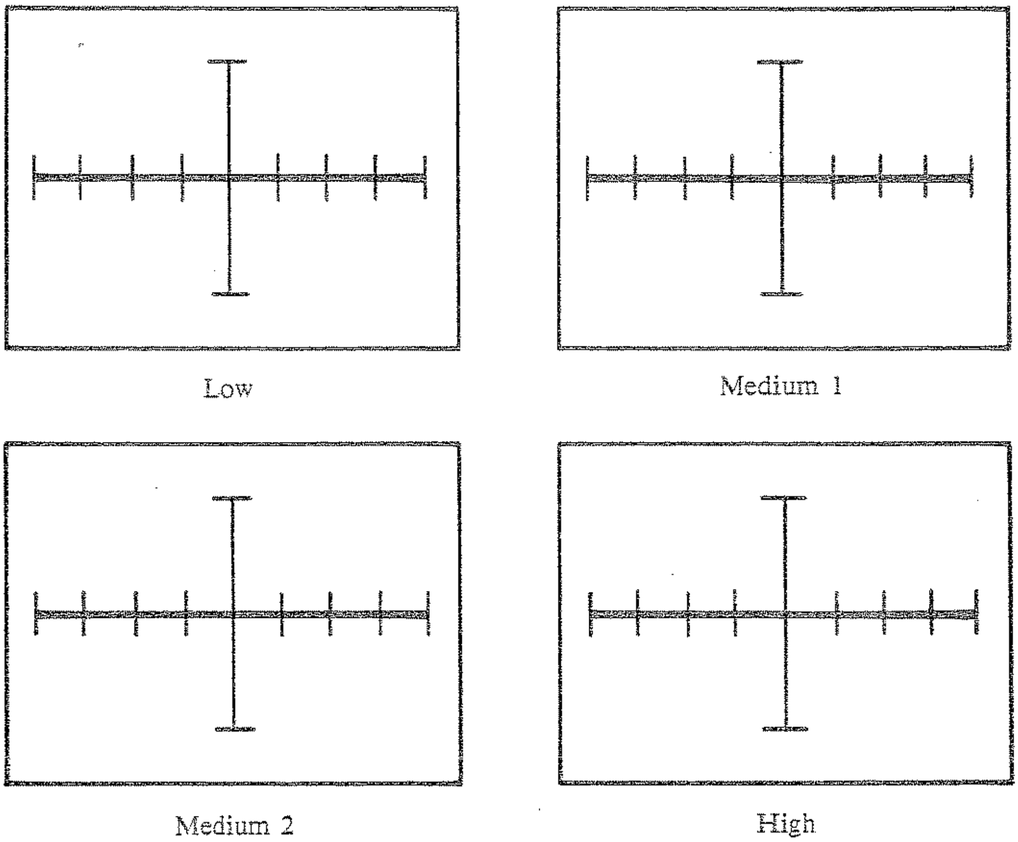


Figure 8-47. Signatures of the Cell (Pin 6 and Pin 5) of a CLM-51 at 60Hz

Testing a CLM-51 with the pulse generator:

The test circuit with the pulse generator for a CLM-51 is shown in Figure 8-48, and its signatures are shown in figure 8-49.

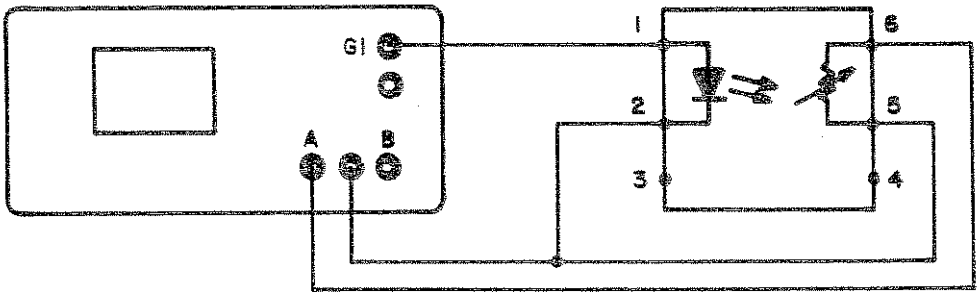


Figure 8-48. Pulse Generator Test Circuit for a CLM-51 Photocell Optocoupler

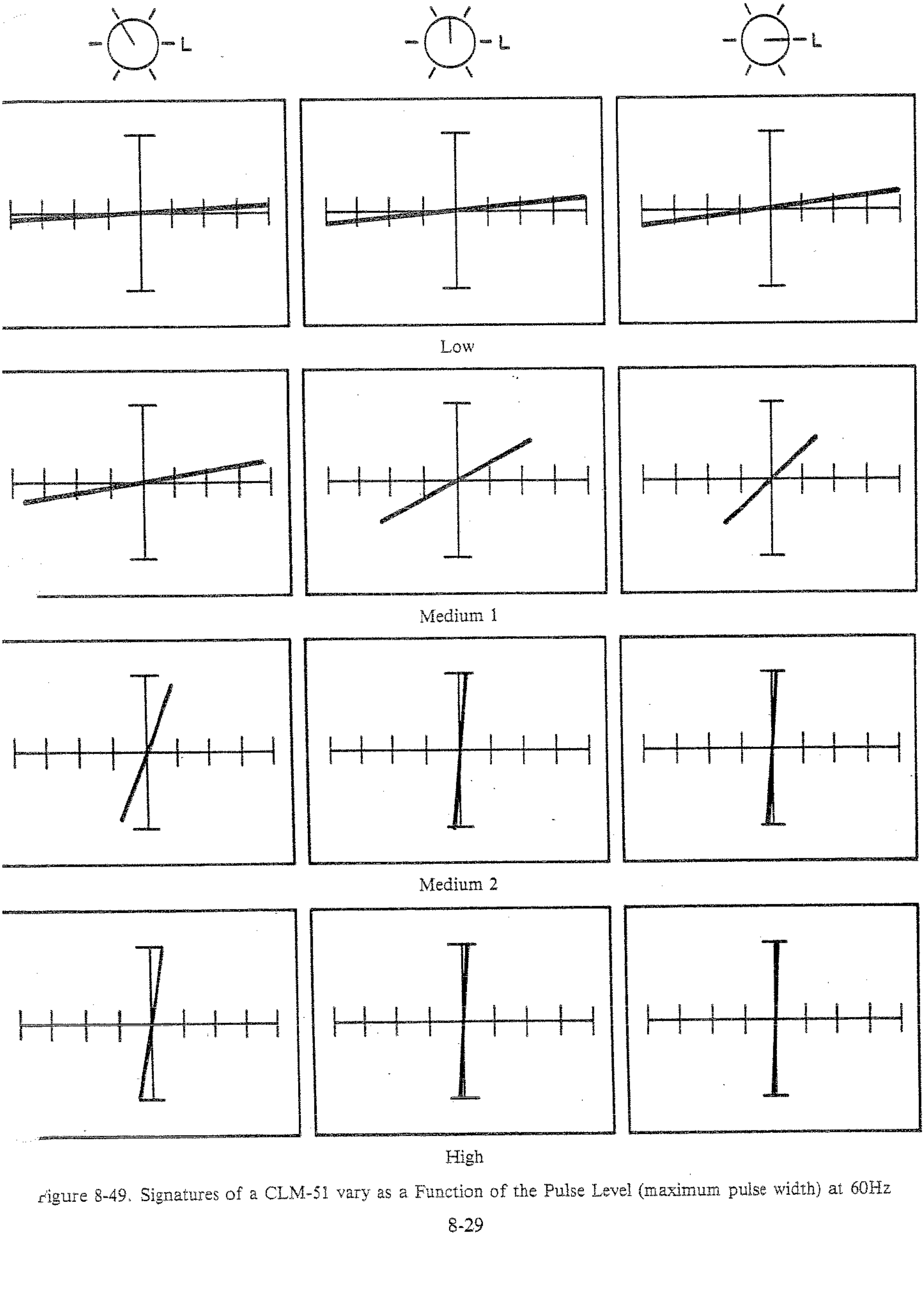


Figure 8-49. Signatures of a CLM-51 vary as a Function of the Pulse Level (maximum pulse width) at 60Hz

SECTION 9
TESTING COMPONENTS BY COMPARISON

9.1 INTRODUCTION

The previous sections of this manual have described the techniques of using the Tracker 2000 to examine good components. This section describes the examination of defective components using the Tracker 2000 in the alternate (comparison) mode.

As described in Section 2, when the alternate button is selected, the Tracker 2000 operates in the alternate mode and will switch from displaying channel A to displaying channel B at a rate set by the rate control. In this mode, the common on a known good circuit or device is connected to the same common on the circuit or device under test. A dissimilarity in the signatures then shows an impedance difference between the known good unit and the unit under test. Refer to Figure 9-1 for Tracker 2000 connections in the alternate mode.

9.2 SETUP PROCEDURES

Set up the Tracker 2000, the known good device, and the device under test as follows:

.. Connect the channel A test lead to a known good device.

2. Connect the channel B test lead to the same node of the device under test.

3. Connect the Tracker 2000 common to the same nodes of the known good device and the device under test.

4. Select the alternate button. The Tracker 2000 circuit will alternately display the signature of the known good device and the device under test. By examining the signature differences, a defective component can be detected.

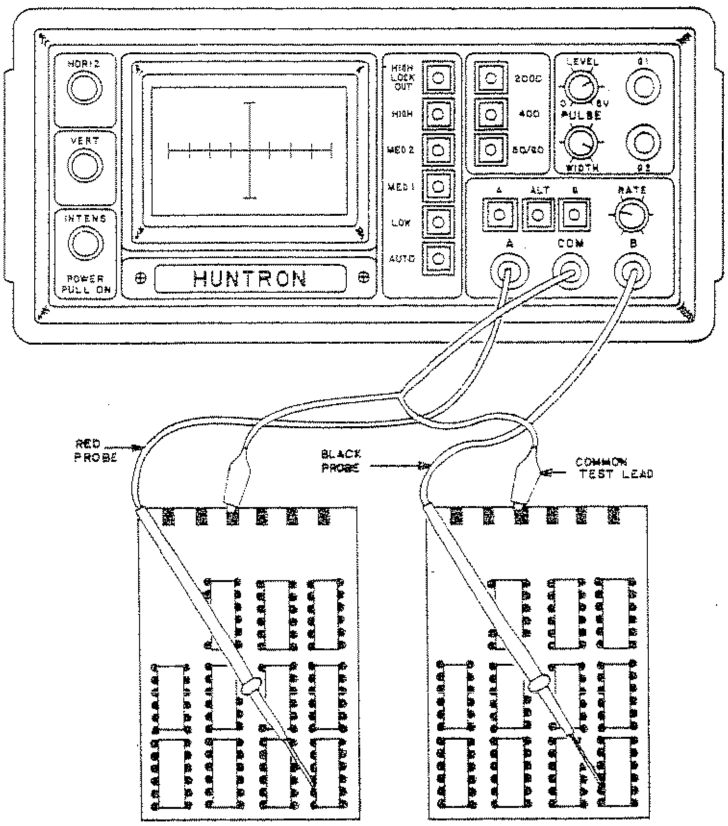


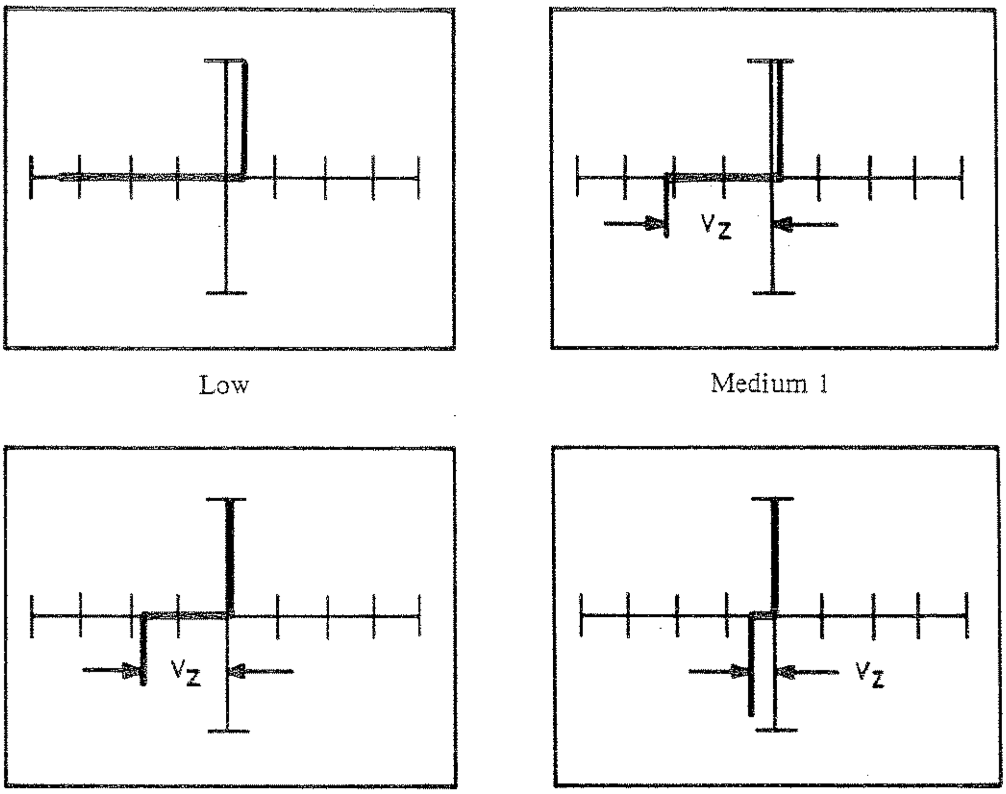
Figure 9-1. Alternate Mode Setup

9.3 POWER TRANSISTOR MJE240

9.3.1 MJE240 B-E Junction

Figure 9-2 shows the signatures of a known good MJE240 using the emitter as the common. This device has a sharp zener voltage (V_Z) across the B-E junction.

Figure 9-3 shows the signatures of a defective MJE240. This device has no zener voltages across the B-E junction in the medium 2 and high ranges.



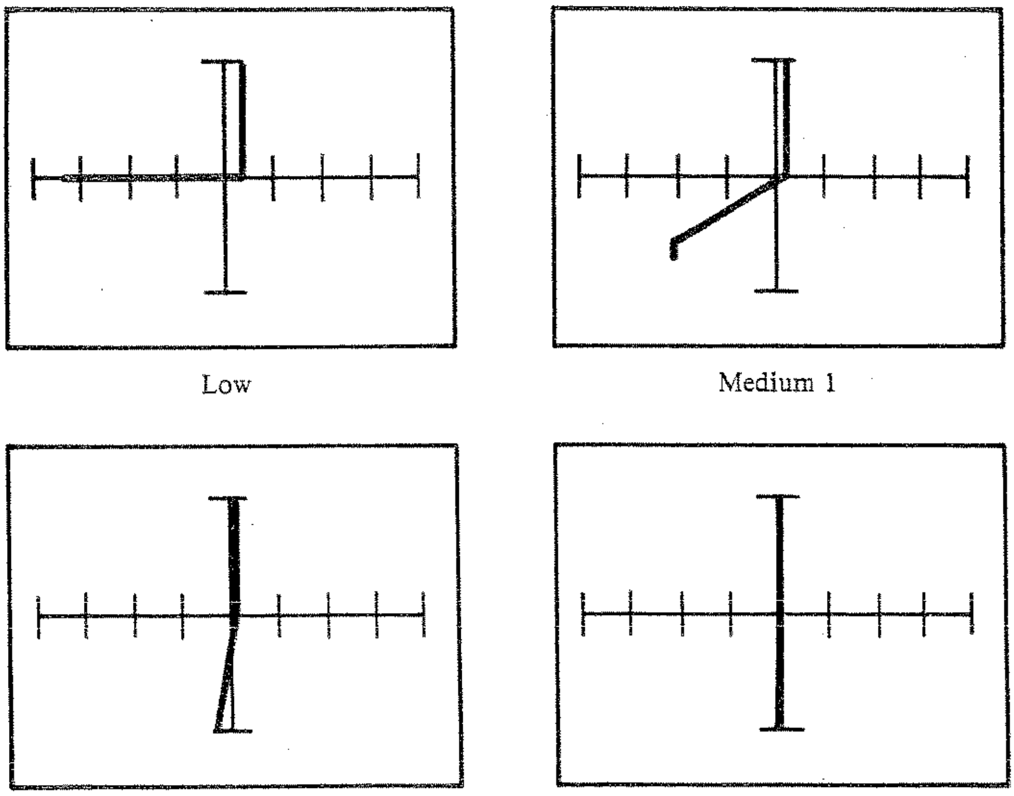
Low

Medium 1

Medium 2

High

Figure 9-2. Signatures Between Base-Emitter of a Good MJE240 Transistor



Low

Medium 1

Medium 2

High

Figure 9-3. Signatures Between Base-Emitter of a Defective MJE240 Transistor

9.3.2 MJE240 C-E Connection

Figure 9-4 shows the signatures of a known good MJE240 using the emitter as common. The MJE240 has a 80 volt C-E breakdown voltage so the right side of the signature (positive half-cycle of the test signal) appears as an open circuit in all ranges. The current leg on the left side of the signature is due to a series connection of C-B junction (forward biased) and the B-E junction (zener breakdown). Since this is an NPN transistor, only the left side (positive C-E voltages) is normally used in most circuits, and the reserve breakdown does not affect anything.

Figure 9-5 shows the signatures of a defective MJE240.

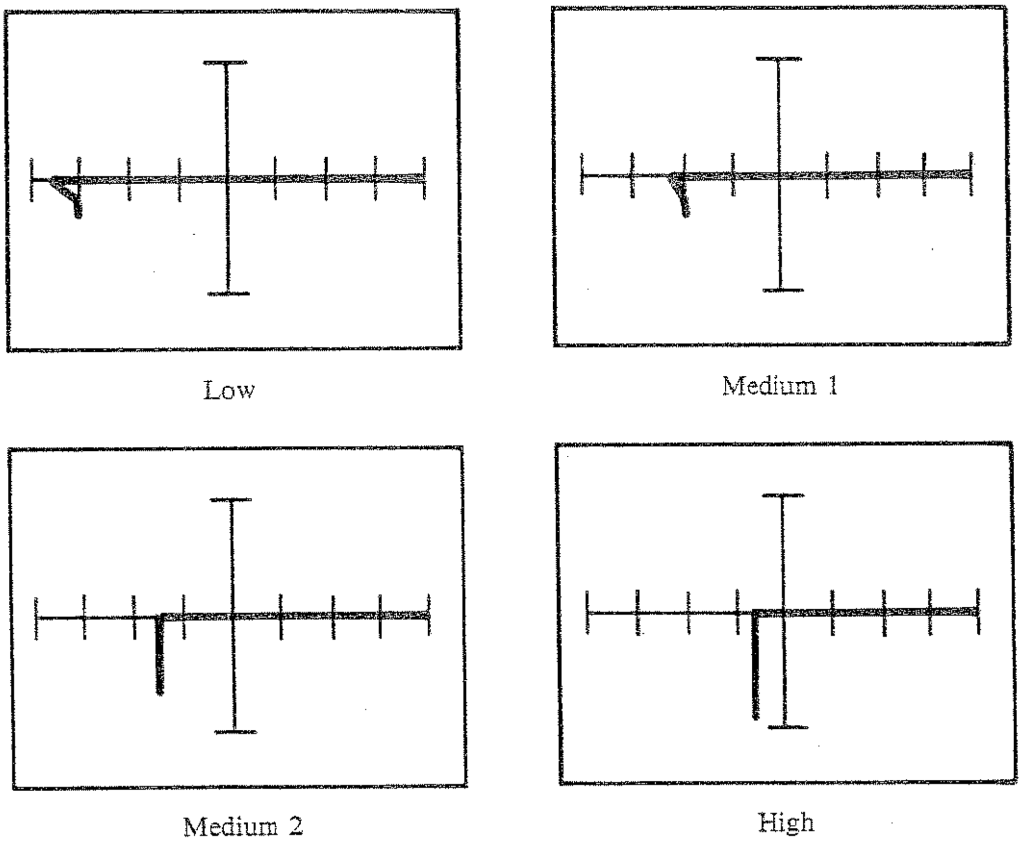


Figure 9-4. Signatures Between Collector-Emitter of a Good MJE240 Transistor

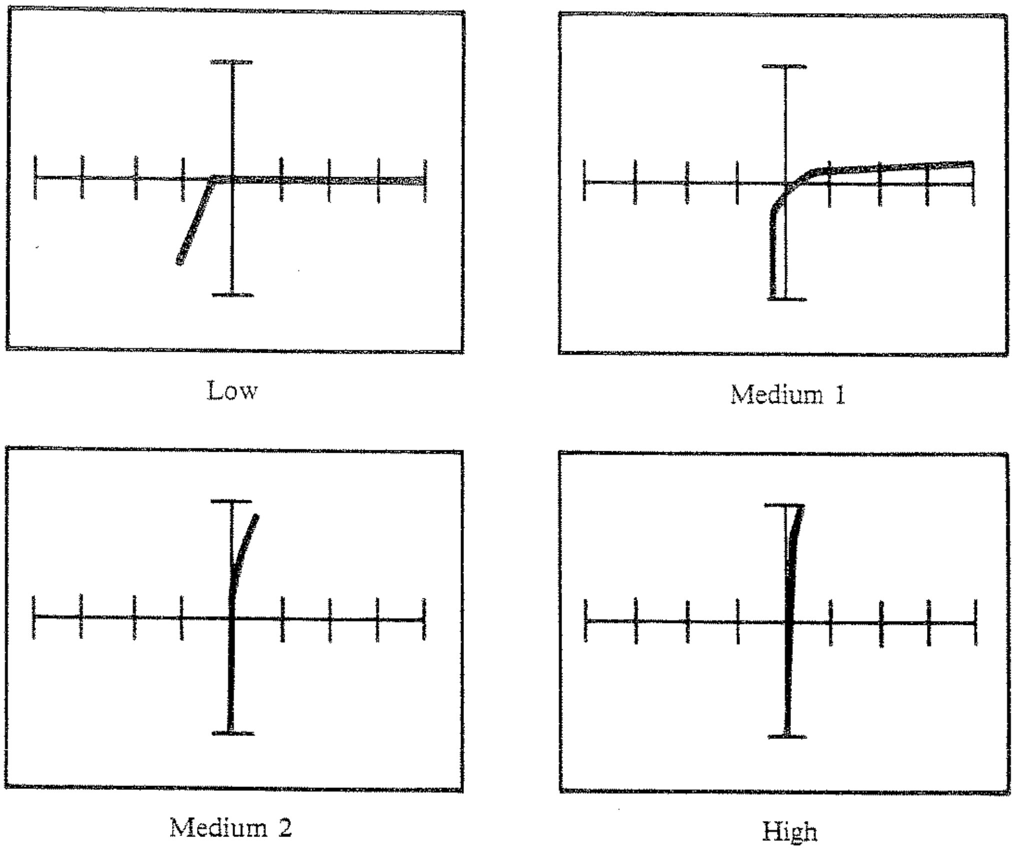


Figure 9-5. Signatures Between Collector-Emitter of a Defective MJE240 Transistor

9.4 HIGH VOLTAGE DIODE HV15F

In this example, there is no signature difference when comparing a known good diode and defective diode in the low range. In the medium 2 and high ranges, the difference is obvious (See Figure 9-6 and 9-7).

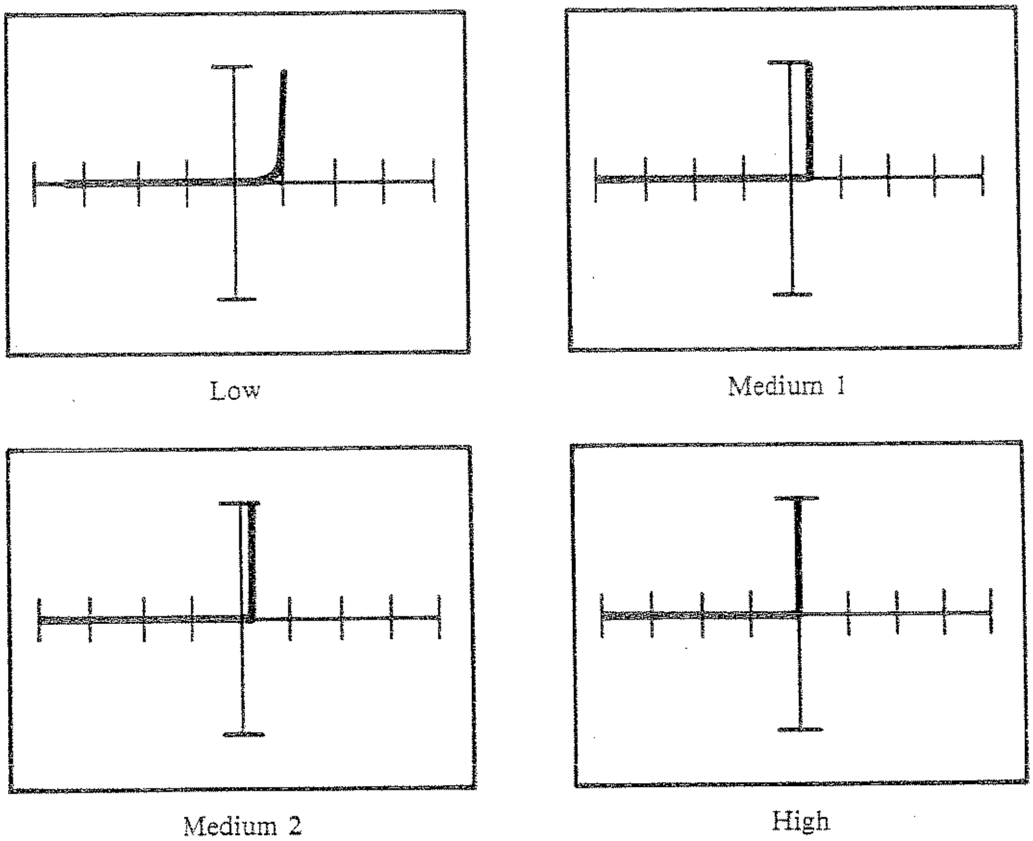


Figure 9-6. Signatures of a Good HV15F Diode

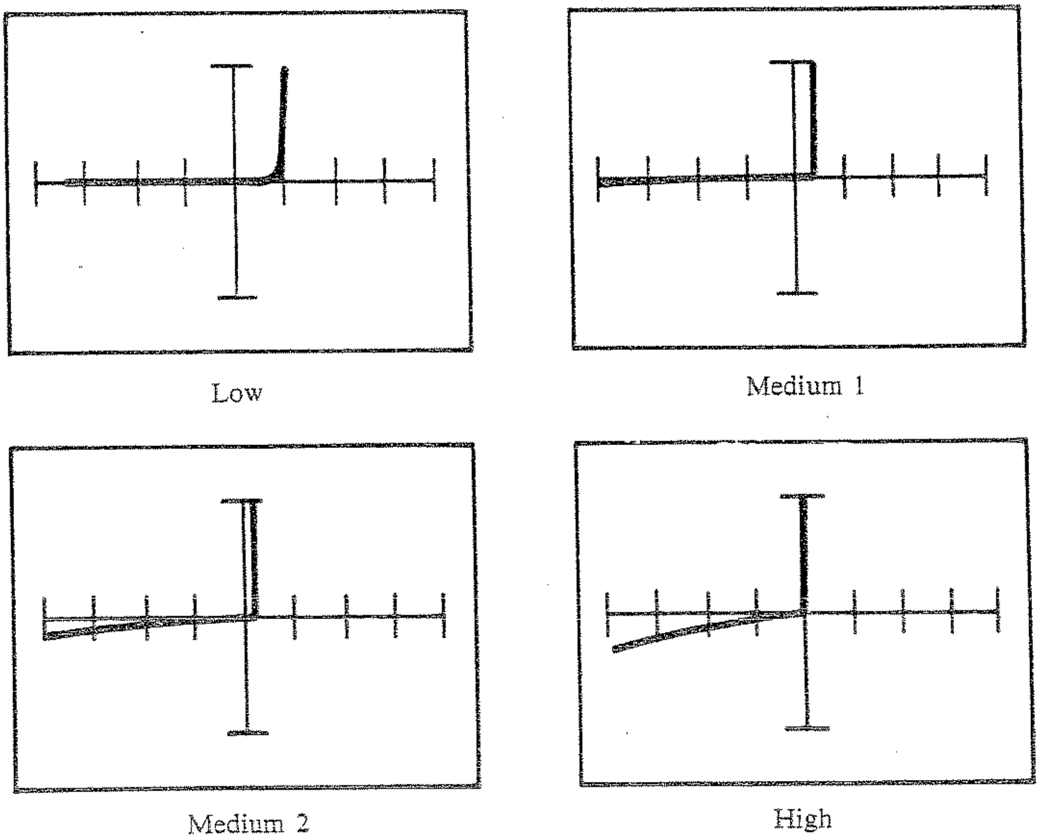
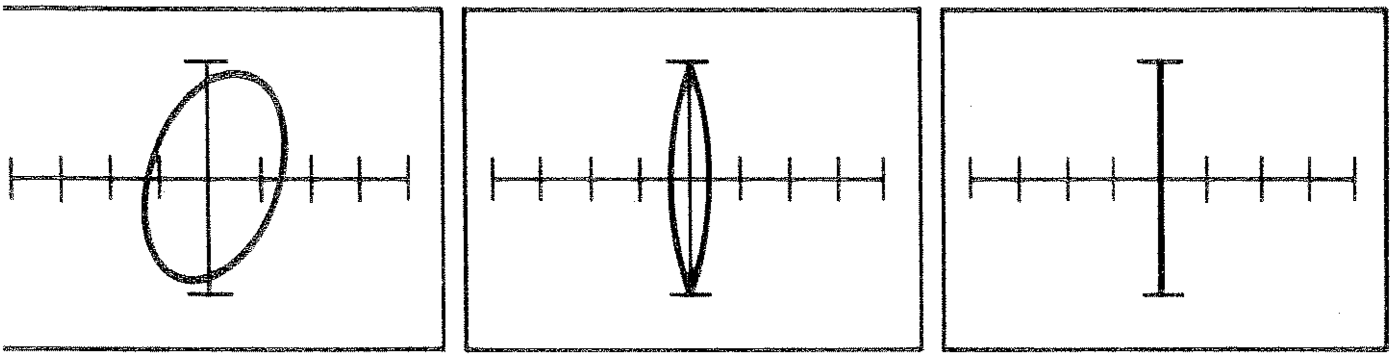


Figure 9-7. Signatures of a defective HV15F Diode

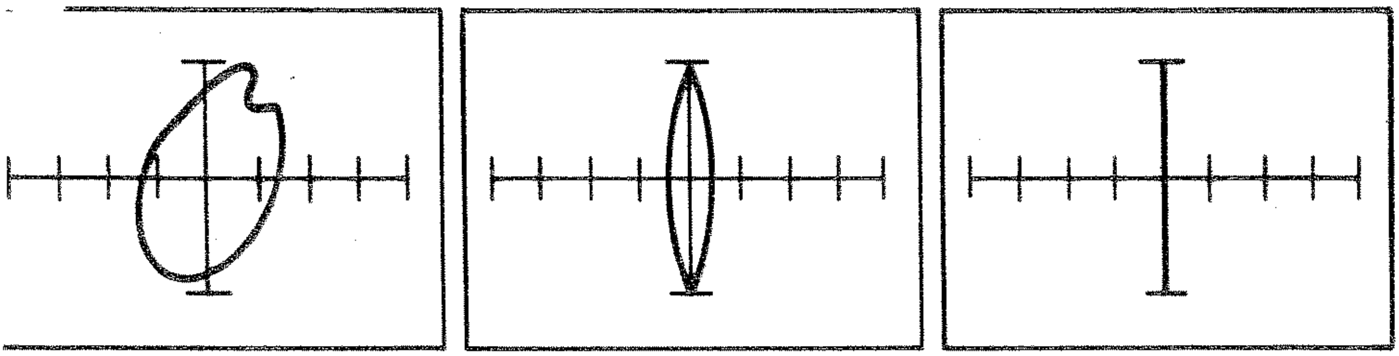
9.5 100uF 25V ELECTROLYTIC CAPACITOR

r a good 100uF capacitor, a smooth ellipse is produced in the low range, while a defective capacitor displays an irregular shape. Figures 9-8 and 9-9 provide a comparison of good to defective capacitors.



Low | Medium 1 | Medium 2/High

Figure 9-8. Patterns of Known Good Capacitor.



Low | Medium 1 | Medium 2/High

Figure 9-9. Patterns of a Defective Capacitor.